

We use the C-ADC of the ADBMS6830B to measure the cell voltages of the battery. The maximum lifetime error for voltage measurement is ± 2 mV, since the maximum voltage of the cell is 4,2 V. (Fig. 1) [1]

SPECIFICATIONS

Specifications apply over the full V_+ operating voltage range and full operating junction temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), unless otherwise noted.

Table 1. C-ADC DC Specifications

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|----------------------|--|-----|------------|--|-------------------|
| MEASUREMENT RESOLUTION | | | | 0.15 | | mV/bit |
| DIFFERENTIAL INPUT RANGE | V_{DIF} | $-0.1 \text{ V} < (C_x \text{ to } V_-) < 80 \text{ V}$ | -2 | | +5.5 | V |
| ADC OFFSET VOLTAGE ¹ | | | | ± 0.1 | | mV |
| ADC GAIN ERROR ¹ | | | | ± 0.01 | | % |
| ADC UPDATE RATE | | | 0.9 | 1 | 1.1 | kHz |
| ADC TRANSITION NOISE | | | | 40 | | $\mu\text{V rms}$ |
| LIFETIME CELL TOTAL MEASUREMENT ERROR | C-TME | $V_{\text{DIF}} \leq \pm 2.0 \text{ V}$ $V_{\text{DIF}} \leq 3.3 \text{ V}$ $V_{\text{DIF}} \leq 4.5 \text{ V}$ $V_{\text{DIF}} \leq 5.5 \text{ V}$ | | | ± 1.5 ± 1.8 ± 2 ± 3 | mV |
| INPUT LEAKAGE CURRENT | | ADC off | 0 | ± 250 | | nA |
| DIFFERENTIAL INPUT RESISTANCE | $R_{\text{IN_ADC}}$ | ADC on | 1.6 | 2.2 | 3 | $M\Omega$ |
| DIFFERENTIAL INPUT RESISTANCE DURING OPEN WIRE DETECTION | | | | 1.75 | | $k\Omega$ |
| ADC SAMPLING FREQUENCY | f_s | | 3.7 | 4.1 | 4.5 | MHz |

¹ The ADC specifications are guaranteed by the total measurement error specification.

Table 2. S-ADC DC Specifications

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|---------------------|---|------|------------------|--------------------|-------------------|
| MEASUREMENT RESOLUTION | | | | 1.5 ¹ | | mV/bit |
| INPUT RANGE | $V_{\text{DIF_S}}$ | $-0.1 \text{ V} < (S_x \text{ to } V_-) < 80 \text{ V}$ | -0.3 | | +5.5 | V |
| ADC OFFSET VOLTAGE ² | | | | ± 0.2 | | mV |
| ADC GAIN ERROR ² | | | | ± 0.03 | | % |
| ADC UPDATE RATE | | | 110 | 125 | 140 | Hz |
| ADC TRANSITION NOISE | | | | 20 | | $\mu\text{V rms}$ |
| S-ADC TOTAL MEASUREMENT ERROR | S-TME | $0 \text{ V} \leq V_{\text{DIF_S}} \leq 4.5 \text{ V}$ $V_{\text{DIF_S}} \leq 5.5 \text{ V}$ | | | ± 7 ± 8 | mV mV |
| INPUT LEAKAGE CURRENT | | ADC off, $V_{\text{DIF_S}} = 5.5 \text{ V}$ | 10 | ± 300 | | nA |
| DIFFERENTIAL INPUT RESISTANCE | | ADC on | 1 | 1.8 | 2.6 | $M\Omega$ |
| DIFFERENTIAL INPUT RESISTANCE DURING OPEN WIRE DETECTION | | | | 20 | | $k\Omega$ |
| GAIN DURING OPEN WIRE DETECTION | | No open wire fault | 85 | 90 | 95 | % |
| ADC SAMPLING FREQUENCY | f_s | | 3.7 | 4.1 | 4.5 | MHz |

¹ The S-ADC result registers are normalized to the weight of the C-ADC results, allowing the same voltage conversion function to be applied. See the register description for more details.

² The ADC specifications are guaranteed by the total measurement error specification.

Figure 1: ADBMS6830B specifications

Reference

[1] Data Sheet ADBMS6830B Rev.0 page 5. analog.com, 01.2024.