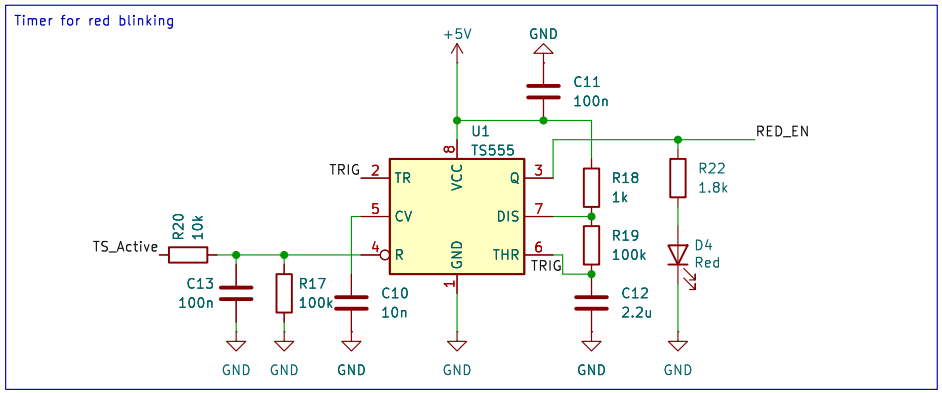
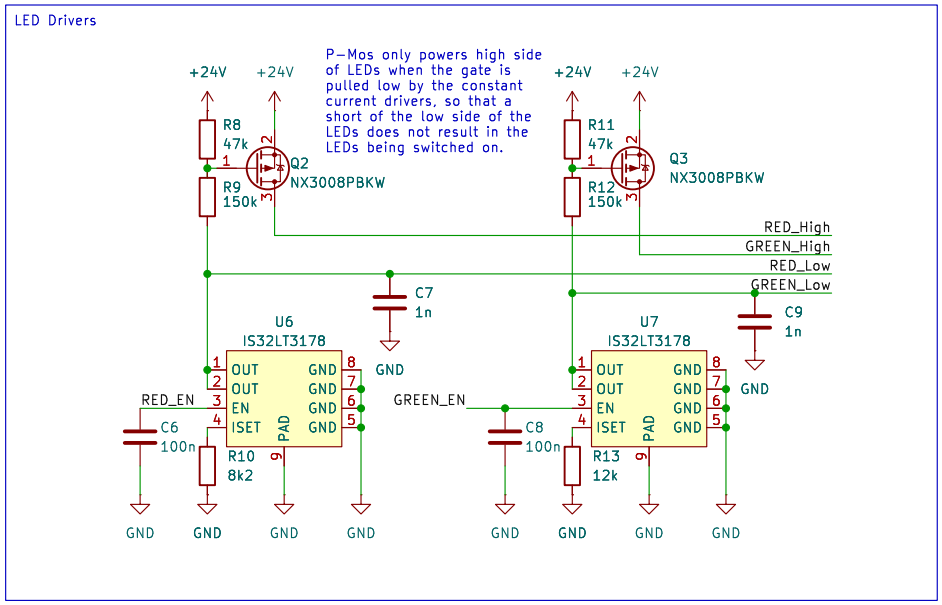
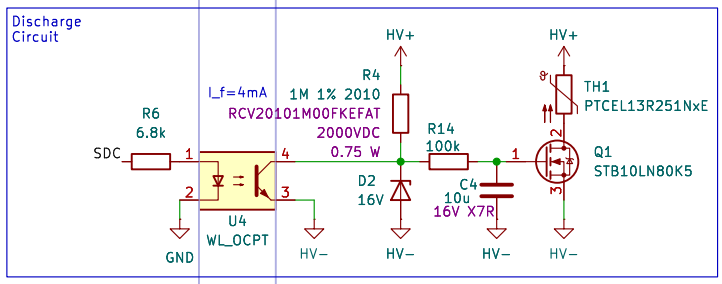
# TSAL driver board and DC-link voltage detection

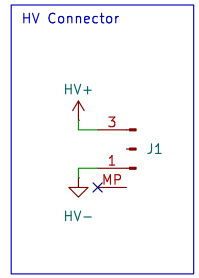
LV

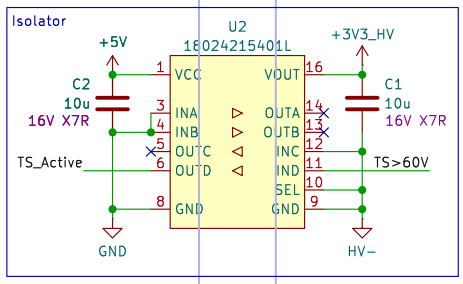
TS

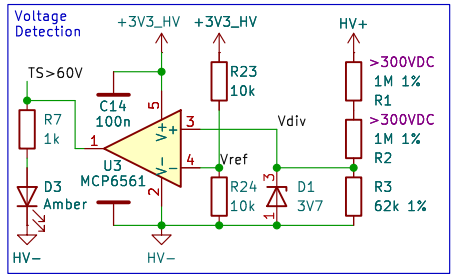


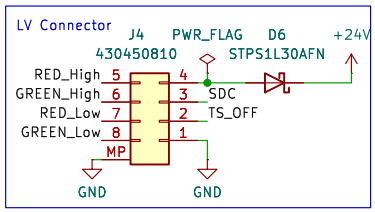



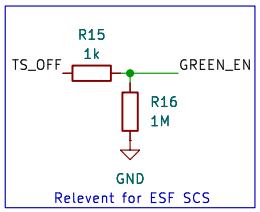



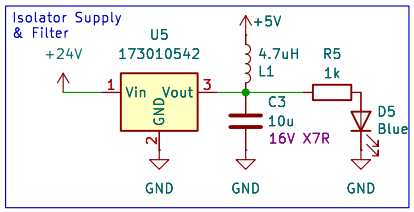




3V7 or 4V. A 3V3 Zener pulls Vdiv down because it allows more current to pass in comparison to the voltage divider. look into it :)

Vref_max = 3.47V * 10.1kΩ / (10.1kΩ + 9.9kΩ) = 1.76V
Vdiv@60V_min = 60V * 61.38Ω / (2*990kΩ + 61.38kΩ) = 1.8V
Vhyst_max@75deg = 6mV < 40mV (1.80V-1.76V)





FASTTUBE

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|---|---|
| **Title: Discharge Circuit** | **Rev: V1** |
| | **Date: 2024-11-10** |
| **Project: DC** | Exp. Date: 2025-05-28 |
| **Author: Karlsson Winkels** | Size: A4 \| Page: 1/1 |