Evaluating the ADBMS6830B, 16-Channel, Battery Stack Monitoring System

FEATURES

▸ Full featured evaluation board for the ADBMS6830B
▸ Demonstrates high-performance measurements of the ADBMS6830B
▸ Included two isoSPI ports for reversible isoSPI support
▸ Daisy-chain capability
▸ Cell and GPIO accessible via optional connectors
▸ isoSPI connections via simple DuraClik™ connectors
▸ Compatible boards
▸ EVAL-ADBMS6822, dual master isoSPI board
▸ EVAL-SDP-CK1Z, controller board
▸ PC software for control and data analysis when used with the Analog Devices, Inc., SDP-K1 microcontroller

EVALUATION KIT CONTENTS

▸ EVAL-ADBMS6830BMSW

DOCUMENTS NEEDED

▸ ADBMS6830B data sheet

EQUIPMENT NEEDED

▸ EVAL-SDP-CK1Z controller board
▸ EVAL-ADBMS6822 dual master isoSPI adapter board

SOFTWARE NEEDED

▸ Evaluation software for the ADBMS6830B
  ▸ BMS Browser\Windows®-based graphical user
  ▸ Interface program
  ▸ Request through:https://form.analog.com/form_pages/softwaremodules/SRF.aspx

GENERAL DESCRIPTION

The evaluation board EVAL-ADBMS6830BMSW features ADBMS6830B, a 16-Channel battery-stack monitor. Multiple boards can be linked through a 2-wire isolated serial port interface (isoSPI™) to monitor a long series of cells in a stack. The evaluation board also features reversible isoSPI, enabling a redundant communication path. The PCB, components, and DuraClik connectors are optimized for low EMI susceptibility and emissions.

The EVAL-ADBMS6830BMSW can communicate to a PC by connecting an EVAL-ADBMS6822 dual master isoSPI together with EVAL-SDP-CK1Z (SDP-K1). The SDP-K1 provides a standard SPI interface, which can be translated to isoSPI by EVAL-ADBMS6822 and then connected to a EVAL-ADBMS6830BMSW isoSPI port (J3 or J4 connector). A separate EVAL-ADBMS6822 companion board provides two SPI-isoSPI channels for reversible operation.

The design files for this circuit board are available.

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REVISION HISTORY

11/2023—Revision 0: Initial Version
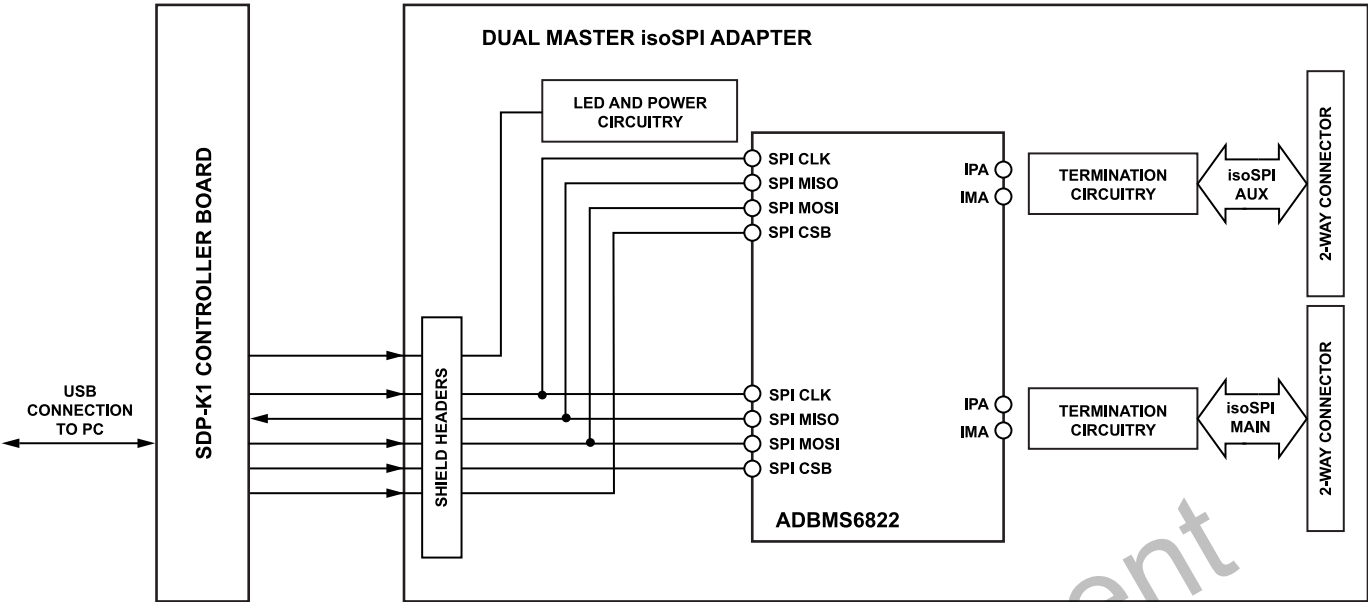
FUNCTIONAL BLOCK DIAGRAMS

Figure 1. Overview of EVAL-ADBMS6822 Dual isoSPI Master Adapter and EVAL-SDP-CK1Z Interface Board (Both sold separately)
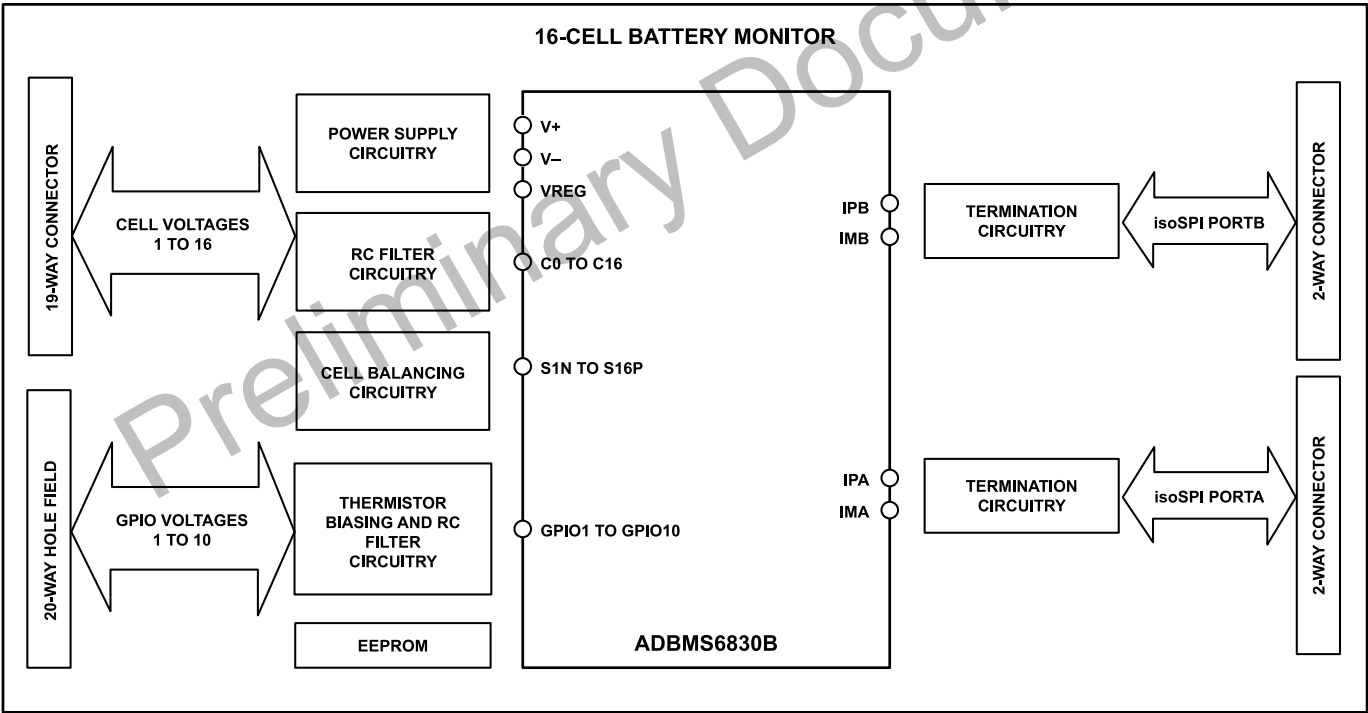

Figure 2. Overview of isoSPI Slave Evaluation Board

EVALUATION BOARD FEATURES

HARDWARE SETUP

Wiring J1 Connector

The EVAL-ADBMS6830BMSW board connection is critical; correct wiring must be followed to avoid the risk of damaging the evaluation board.

When connected to a battery stack, the cell group being monitored provides power for the EVAL-ADBMS6830BMSW . To connect the cell group, separate the screw-terminal block section from the J1 connector. Then, insert the cell-voltage connections or resistors into the screw-terminal clamping contacts. These connections provide the power and input stimuli for the battery stack monitor IC.

The cell voltages are wired to J1, starting from position 1 (the most negative potential of the group). The appropriate evaluation board J1 connection pin-out is shown in Table 1.

Alternatively, resistors can be used to simulate battery cell voltages. 100 Ω ½ W or equivalent resistors are recommended because 100 Ω (or lower values) typically will not induce measurement errors, and the ½ W (or greater rating) will keep the resistor temperatures low, preventing power dissipation damage.

EVAL-ADBMS6830BMSW 16 Resistor Connection

Carefully connect 16 100 Ω resistors onto the screw-terminal block between each CPIN input clamping contact from position 1 to position 17, as shown in Table 1, EVAL-ADBMS6830BMSW J1 pinout, Figure 3, and the resistor divider string. Provide a stack-equivalent power supply connection to position 17 (positive) and position 1 (negative). The power supply may be adjusted to provide the desired nominal cell voltage (for example, 52.8 V will be 3.3 V per cell).
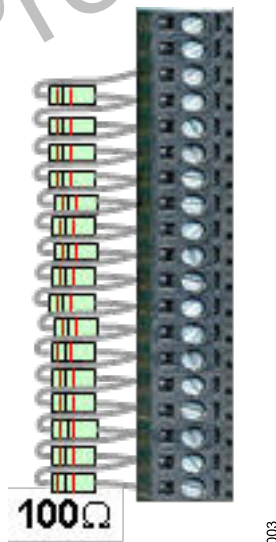

Figure 3. Typical 16-Cell Resistor Divider String Connection

Table 1. Pin Designations for the J1 Sixteen Way Connector

Pin No.	Connection
1	C0 (stack-)
2	C1
3	C2
4	C3
5	C4
6	C5
7	C6
8	C7
9	C8
10	C9
11	C10
12	C11
13	C1
14	C13
15	C14
16, 17	C15C16 (stack+)

JUMPERS

There are no jumpers to configure on the EVAL-ADBMS6830BMSW.

EVAL-ADBMS6830BMSW SERIAL INTERFACE OPTIONS

isoSPI is the only communication option for the EVAL-ADBMS6830BMSW. Due to the custom EMI-optimized isoSPI cable with DuraClik connectors, it is highly recommended to use the EVAL-ADBMS6822 dual master isoSPI demo board or equivalent for easy plug-and-play operation. The EVAL-ADBMS6822 dual master isoSPI demo board can be connected as a typical single-ended isoSPI bus master or to both ends of a reversible configuration with two isoSPI bus masters. Refer to the demo manual EVAL-ADBMS6822 for usage details.

EVAL-ADBMS6830BMSW OPTIONAL CONNECTIONS

GPIO Optional Header J5

This double row of thru-holes (hole field) can be used as test points for GPIO voltages or can be wired with individual V-/GND connections with each GPIO.

Table 2. Pin Designations for the J5 Twenty Way Connector

Pin No.	Connection
1	GPIO1
2	GPIO2
3	GPIO3
4	GPIO4
5	GPIO5
6	GPIO6
7	GPIO7

EVALUATION BOARD FEATURES

Table 2. Pin Designations for the J5 Twenty Way Connector (Continued)

Pin No.	Connection
8	GPIO8
9	GPIO9
10	GPIO10
11	V⁻
12	V⁻
13	V⁻
14, 15, 16, 17, 18, 19, 20	V⁻, V⁻, V⁻, V⁻, V⁻, V⁻, V⁻

IREG Optional Header J2

This pair of thru-holes can be used to measure IREG with an ammeter. The use of an ammeter bypasses the D2 LED (VREG active), which allows accurate measurement of IREG current. Add an ammeter between J2 pins 1 and 2 to measure IREG.

SUPPLY Optional Header J6

This pair of thru-holes can be used to insert or measure the supplied voltage with a power supply or voltmeter, respectively. To furnish power separately from the cell stack, remove R55 and the power board using J6.

EVAL-ADBMS6822 TO EVAL-ADBMS6830BMSW TYPICAL ISOSPI CONNECTION

A typical isoSPI connection begins with the isoSPI master connected to the first (or bottom) EVAL-ADBMS6830BMSW. Additional EVAL-ADBMS6830BMSW boards can be daisy-chained onto the isoSPI bus. Communication begins with the first (or bottom) EVAL-ADBMS6830BMSW, then to the next upper EVAL-ADBMS6830BMSW, and finally, to the last (or top) EVAL-ADBMS6830BMSW.

Figure 4 shows the following connections for two boards on a stack interfaced to a PC:

1. Connect the EVAL-ADBMS6822 dual master isoSPI demo board to the EVAL-SDP-CK1Z (referred to hereafter as SDP-K1 and labeled as such).

   a. Connect the EVAL-ADBMS6822 board directly onto the shield headers of the SDP-K1.
   b. Set the P14 jumper of the SDP-K1 to the 3.3V position.
2. Connect a USB cable from the PC USB port to the SDP-K1 P2 connector.
3. Connect the EVAL-ADBMS6822 to the EVAL-ADBMS6830BMSW. This EVAL-ADBMS6830BMSW is the first (or bottom) board of the stack.

   a. Connect a 2-wire twisted-pair patch cable from the EVAL-ADBMS6822 J1 MAIN DuraClik connector to the bottom EVAL-ADBMS6830BMSW J3 isoSPI A DuraClik connector.

4. Connect or daisy-chain the EVAL-ADBMS6830BMSW to another EVAL-ADBMS6830BMSW in isoSPI mode. This EVAL-ADBMS6830BMSW is the last (or top) board of a two-board stack. More EVAL-ADBMS6830BMSW upper boards can be daisy-chained together in the same manner.

   a. Connect a 2-wire twisted-pair patch cable from the bottom EVAL-ADBMS6830BMSW J4 isoSPI B DuraClik connector to the next upper or top.
5. CAUTION! Prevent damage to the EVAL-ADBMS6830BMSW. See Table 1 and confirm that the cell-voltage connections to the screw-terminal block match the EVAL-ADBMS6830BMSW J1 pin-out.
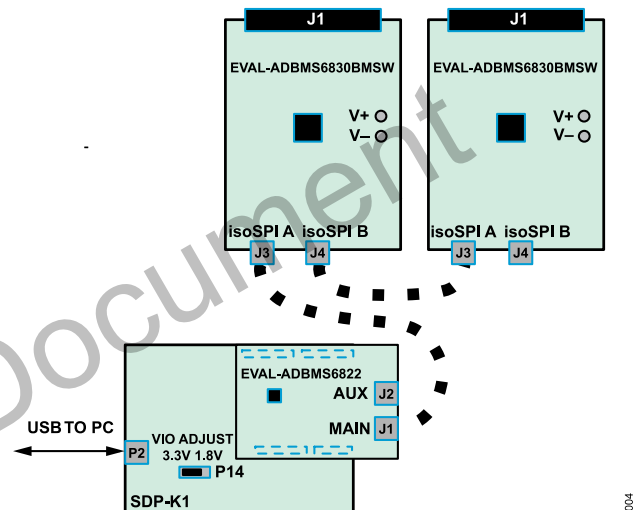

Figure 4. EVAL-ADBMS6830BMSW Typical isoSPI Connection to the Bottom EVAL-ADBMS6830BMSW in a Two-Board EVAL-ADBMS6830BMSW Stack

   a. Plug the screw-terminal block(s) into the J1 cell-voltage connector(s).
6. A Windows-based graphical user interface is available. Refer to the BMS Browser Software Manual to properly set up the PC with the BMS browser software to allow communication to the EVAL-ADBMS6830BMSW boards. Refer to the Where To Get The BMS Browser Software?? of this demo manual to request this software.

CAUTION:

▶ The 2-wire twisted-pair patch cable with the DuraClik end plugs have 1 mm thick center locking tabs on the wiring side that must be pressed down to release from the DuraClik receptacles. Failure to do so may damage the cable and prevent board-to-board isoSPI communication.

EVALUATION BOARD FEATURES

EVAL-ADBMS6822 TO EVAL-ADBMS6830BMSW REVERSE ISOSPI CONNECTION

A reverse isoSPI connection begins with the isoSPI master connected to the last (or top) EVAL-ADBMS6830BMSW. Additional EVAL-ADBMS6830BMSW boards can be daisy-chained onto the isoSPI bus. Communication begins from the last (or top) EVAL-ADBMS6830BMSW then to the next lower EVAL-ADBMS6830BMSW and, finally, to the first (or bottom) EVAL-ADBMS6830BMSW.

Figure 5 shows the following connections for two boards on a stack interfaced to a PC:

1. Connect the EVAL-ADBMS6822 dual master isoSPI demo board to the SDP-K1.

    a. Connect the EVAL-ADBMS6822 board directly onto the shield headers of the SDP-K1.

    b. Set the P14 jumper of the SDP-K1 to the 3.3V position.

2. Connect a USB cable from the PC USB port to the SDP-K1 P2 connector.

3. Connect the EVAL-ADBMS6822 to the EVAL-ADBMS6830BMSW in isoSPI mode. This EVAL-ADBMS6830BMSW is the last (or top) board of a two-board stack.

    a. Connect a 2-wire twisted-pair patch cable from the EVAL-ADBMS6822 J1 MAIN DuraClik connector to the top EVAL-ADBMS6830BMSW J4 isoSPI B DuraClik connector.

4. Connect or daisy-chain the EVAL-ADBMS6830BMSW to another EVAL-ADBMS6830BMSW in isoSPI mode. This EVAL-ADBMS6830BMSW is the first (or bottom) board of a two-board stack. More EVAL-ADBMS6830BMSW lower boards can be daisy-chained together in the same manner.

    a. Connect a 2-wire twisted-pair patch cable from the top EVAL-ADBMS6830BMSW J3 isoSPI A DuraClik connector to the next lower or bottom EVAL-ADBMS6830BMSW J4 isoSPI B DuraClik connector.
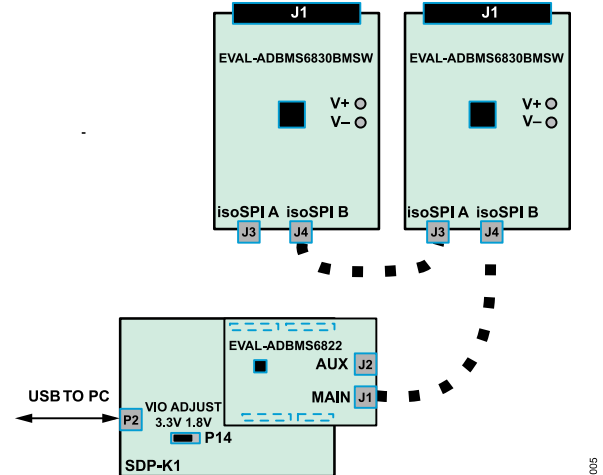

Figure 5. EVAL-ADBMS6830BMSW Reverse isoSPI Connection to the Top EVAL-ADBMS6830BMSW in a Two-Board EVAL-ADBMS6830BMSW Stack

5. CAUTION! Prevent damage to the EVAL-ADBMS6830BMSW. See Table 1 and confirm that the cell-voltage connections to the screw-terminal block matches the EVAL-ADBMS6830BMSW J1 pinout.

    a. Plug the screw-terminal block(s) into the J1 cell-voltage connector(s).

6. A Windows-based graphical user interface is available. Refer to the BMS Browser Software Manual to properly setup the PC with the BMS Browser software to allow communication to the EVAL-ADBMS6830BMSW boards. Refer to the Where To Get The BMS Browser Software?? of this demo manual to request this software.

CAUTION:

▶ The 2-wire twisted-pair patch cable with the DuraClik end plugs have 1mm thick center locking tabs on the wiring side that must be pressed down to release from the DuraClik receptacles. Failure to do so may damage the cable and prevent board-to-board isoSPI communication.

EVALUATION BOARD FEATURES

EVAL-ADBMS6822 TO EVAL-ADBMS6830BMSW REDUNDANT ISOSPI CONNECTION

A redundant isoSPI connection begins with the primary (or main) isoSPI master connected to the first (or bottom) EVAL-ADBMS6830BMSW and has a backup auxiliary (or aux) isoSPI master connected to the last (or top) EVAL-ADBMS6830BMSW. Additional EVAL-ADBMS6830BMSW[1] boards can be daisy-chained between the two isoSPI masters on the isoSPI bus. Primary (or main) communication begins with the first (or bottom) EVAL-ADBMS6830BMSW then to the next upper EVAL-ADBMS6830BMSW and finally, to the last (or top) EVAL-ADBMS6830BMSW. The backup auxiliary (or aux) communication begins in the reverse direction to provide coverage when a possible isoSPI daisy-chain break occurs shows the following connections for two boards on a stack interfaced to a PC:

1. Connect the EVAL-ADBMS6822 dual master isoSPI demo board to the SDP-K1.

    a. Connect the EVAL-ADBMS6822 board directly onto the shield headers of the SDP-K1.
    b. Set the P14 jumper of the SDP-K1 to the 3.3V position.
2. Connect a USB cable from the PC USB port to the SDP-K1 P2 connector.
3. Connect the EVAL-ADBMS6822 primary (or main) isoSPI master to the first (or bottom) EVAL-ADBMS6830BMSW board of the stack.

    a. Connect a 2-wire twisted-pair patch cable[2] from the EVAL-ADBMS6822 J1 MAIN DuraClik connector to the bottom EVAL-ADBMS6830BMSW J3 isoSPI A DuraClik connector.
4. Connect or daisy-chain the EVAL-ADBMS6830BMSW to another EVAL-ADBMS6830BMSW in isoSPI mode. This EVAL-ADBMS6830BMSW is the last (or top) board of a two-board stack. More EVAL-ADBMS6830BMSW upper boards can be daisy-chained together in the same manner.

    a. Connect a 2-wire twisted-pair patch cable[2] from the bottom EVAL-ADBMS6830BMSW J4 isoSPI B DuraClik connector to the next upper or top EVAL-ADBMS6830BMSW J3 isoSPI A DuraClik connector.
5. Connect the EVAL-ADBMS6822 auxiliary (or aux) isoSPI master to the last (or top) EVAL-ADBMS6830BMSW board of the stack.

    a. Connect a 2-wire twisted-pair patch cable[2] from the EVAL-ADBMS6822 J2 AUX DuraClik connector to the top EVAL-ADBMS6830BMSW J4 isoSPI B DuraClik connector.
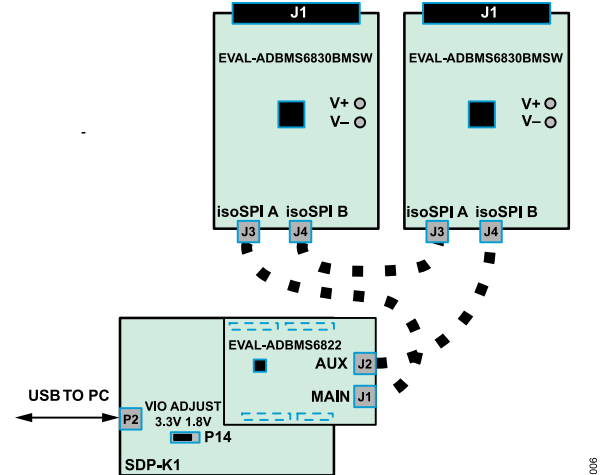

Figure 6. Redundant isoSPI Connection to the Bottom EVAL-ADBMS6830BMSW and Top EVAL-ADBMS6830BMSW in a Two-Board EVAL-ADBMS6830BMSW Stack

6. CAUTION! Prevent damage to the EVAL-ADBMS6830BMSW. See Table 1 and confirm that the cell-voltage connections to the screw-terminal block matches the EVAL-ADBMS6830BMSW J1 pinout.

    a. Plug the screw-terminal block(s) into the J1 cell-voltage connector(s).
7. A Windows-based graphical user interface is available. Refer to the BMS Browser Software Manual to properly setup the PC with the BMS browser software to allow communication to the EVAL-ADBMS6830BMSW boards. Refer to the Where To Get The BMS Browser Software?? of this demo manual to request this software.

CAUTION:

▶ The 2-wire twisted-pair patch cable with the DuraClik end plugs have 1 mm thick center locking tabs on the wiring side that must be pressed down to release from the DuraClik receptacles. Failure to do so may damage the cable and prevent board-to-board isoSPI communication.

EVALUATION BOARD SOFTWARE

WHERE TO GET THE BMS BROWSER SOFTWARE?

Request the GUI software with the **ADI Software Request Form** from the following link:

▶ https://form.analog.com/form_pages/softwaremodules/SRF.aspx
▶ Or search for **Software Request Form** at https://www.ana-log.com.

Preliminary Document

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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