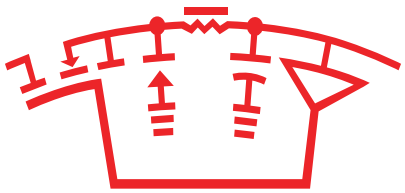

Power Supply Design Seminar

Phase-Shifted Full-Bridge Converter Fundamentals

Texas Instruments

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Topic 4
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The phase-shifted full-bridge converter (PSFB) is common in high-performance power supplies with fast transient response, high power density and high converter efficiency. This topic reviews PSFB operation principles, characteristics of the PSFB, different types of rectifiers, clamp options, converter control modes, synchronous rectifier operation modes and light-load management options. A PSFB design based on the Modular Hardware-System-Common Redundant Power Supply (M-CRPS) base specification demonstrates the ability of a PSFB – with an active clamp circuit – to achieve a high-power design with a high transient response.

Introduction

Today's power-conversion systems demand high efficiency, high power density and lighter weight. In telecommunication, server and PC applications, the 80 Plus certification program has defined efficient power-supply standards for over 15 years. Recently, the Open Compute Project (OCP) announced the M-CRPS specification for server power-supply units (PSUs), which requires even higher efficiency requirements than 80 Plus, as shown in **Table 1**.

Efficiency at	10% load	20% load	50% load	100% load	Note
80 Plus Titanium	90%	94%	96%	91%	@230-V_{AC} input
M-CRPS (<2,500 W)	90%	94%	96%	92%	@240-V_{AC} input
M-CRPS (≥2,500 W)	90%	94%	96%	94%	@240-V_{AC} input

Table 1. *Efficiency requirements of 80 Plus Titanium 230-V internal redundant PSUs and M-CRPS.*

Part of the reason why a PSU needs to have higher efficiency is because of the need for energy-efficient data centers. In data centers less than a decade old, the power usage effectiveness (PUE) is about 3, where PUE is defined in **Equation 1** as:

$$\text{PUE} = \frac{\text{Total\_Datacenter\_Power}}{\text{Actual\_IT\_Power}} \quad (1)$$

The lower the PUE, the more efficient the data center.

Figure 1 and **Figure 2** break down the power consumption of two data centers with a PUE equal to 3 and 1.25, respectively. For the data center with the PUE equal to 3, because a large portion of total data center power is powering the cooling system, increasing server PSU efficiency will definitely help reduce the cooling power needed, reducing the PUE and increasing efficiency.

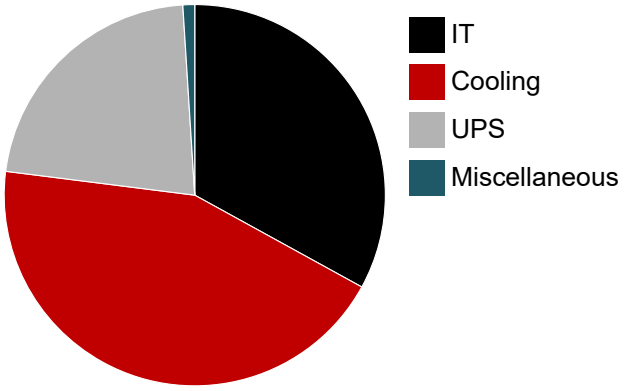

Figure 1. *Data center (PUE = 3) power consumption breakdown.*

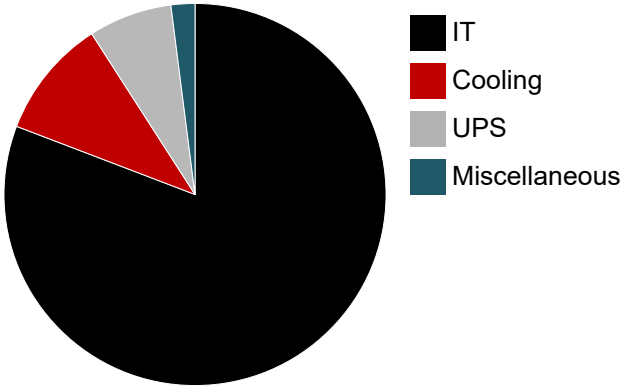

Figure 2. *Data center (PUE = 1.25) power consumption breakdown.*

Not only is higher efficiency mandatory, but server PSUs must deliver more power in a smaller footprint given the emergence of artificial intelligence (AI) and edge computing, along with the continuation of Moore's law. Server loads including the CPU and graphics processing unit (GPU) require much more power, as the transistors per process unit are increasing exponentially. While server rack size remains the same, server PSUs must

have higher power density to meet server load power demands.

High power density is also a requirement for automotive and aerospace applications, as lighter weight means that transportation carriers will have better energy efficiency.

Inside the PSU, one way to reduce weight is to increase the converter switching frequency, which then reduces the magnetic volt-seconds and therefore its size. **Figure 3** plots transformer volume versus switching frequency. An onboard charger with a DC/DC converter switching frequency of 500 kHz will have a transformer with less than half the volume of a 100-kHz transformer.

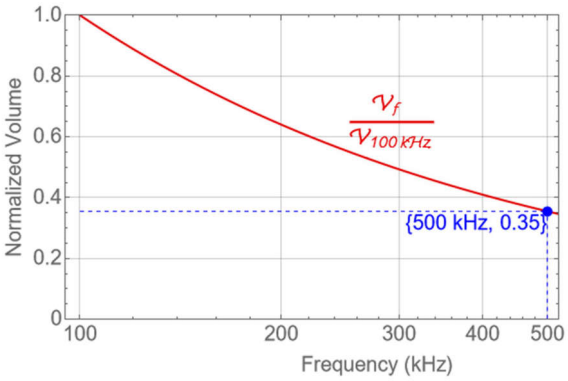

Figure 3. *Transformer volume vs. switching frequency.*

Because the goal is to have higher power density without compromising efficiency, it is essential to introduce soft switching in the PSU to reduce switching losses. Hard-switched converters were first developed in switch-mode power supplies, which have metal-oxide semiconductor field-effect transistor (MOSFET) current and voltage overlapping at the MOSFET turnon transient, as shown in **Figure 4**. A higher switching frequency means more frequent hard-switching transients, and therefore more switching losses. Although it is possible to reduce switching losses by increasing the turnon speed to reduce the overlapped area, a higher voltage-changing slew rate will result in higher noise and electromagnetic interference levels. On the other hand, allowing the negative drain-to-source current to discharge the MOSFET output capacitor (C_{oss}) voltage before the gate voltage goes high does achieve soft-switched turnon, as shown in **Figure 5**. The lack of current and voltage overlap at the MOSFET turnon transient results in no turnon switching losses, which allows the PSU to operate at a high switching frequency and maintain high efficiency at the same time.

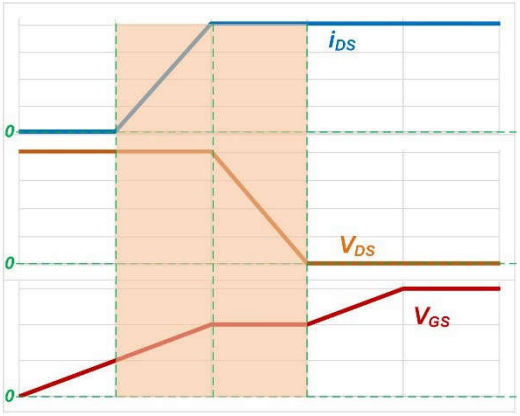

Figure 4. *MOSFET hard-switching turnon transient.*

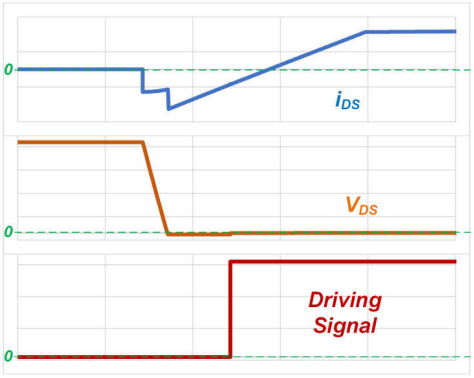

Figure 5. *MOSFET soft-switching turnon transient.*

The same topology with a different control method could result in different behaviors at MOSFET switching transients. Take the full-bridge converter in **Figure 6** as an example. If you were to operate the full-bridge converter with pulse-width modulation (PWM) control, the converter would exhibit hard switching behavior at the MOSFET turnon transient; the MOSFET drain-to-source current starts from positive at the turnon transient.

Figure 7 shows the most significant hard-switched full-bridge converter MOSFET voltage and current waveforms, where nonzero voltage and current overlap at the switching transient, as highlighted by the

green dashed-line circle. When operating the full-bridge converter with phase-shift control between the two input legs, a negative drain-to-source current during the MOSFET turnon transient will avoid nonzero voltage current overlapping for soft switching, as shown in Figure 8.

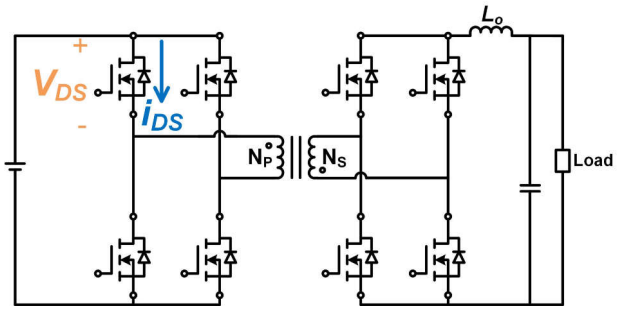

Figure 6. *Full-bridge converter.*

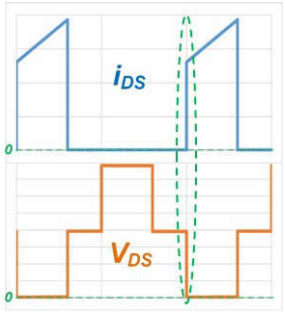

Figure 7. *Hard-switched full-bridge MOSFET current and voltage.*

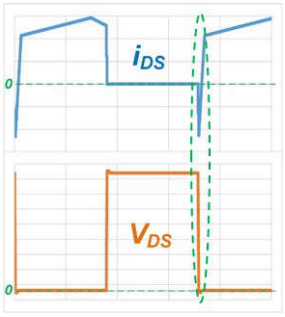

Figure 8. *PSFB MOSFET current and voltage.*

A PFSB converter, inductor-inductor-capacitor (LLC) series resonant converter (SRC) and dual active bridge (DAB) converter can all achieve soft switching, but with different characteristics. An LLC-SRC uses frequency modulation for voltage regulation, while a PSFB and DAB both use phase-shift control with a fixed switching frequency for voltage regulation. An LLC-SRC is the only converter among these three that can achieve soft switching on the output rectifier; it usually has higher peak efficiency than the PSFB or DAB in most cases.

An LLC-SRC isn't a good option for applications with wide input or output ranges, however. For an LLC-SRC to cover wide input or output ranges, you will have to decrease the ratio of the transformer magnetizing inductance to the resonant inductance, which will result in an efficiency reduction. A PSFB and DAB can cover wide input or output ranges with a wide effective duty-cycle (D_{eff}) range without as much of an efficiency reduction penalty as an LLC-SRC. Moreover, peak current-mode control for a PSFB is more mature than current-mode control in an LLC-SRC for fast response to load transients. A PSFB is also the preferred choice in applications with fast transient response requirements. PSFB applications include server PSUs for AI and edge computing with fast load transients as well as battery charger applications, including electric vehicle 400-V, 800-V to 12-V battery power-conversion systems with wide input and output ranges.

In this topic, we will describe the fundamentals of a PSFB including operational principles, rectifier options, clamping options and different types of controls, along with a design example.

PSFB Operational Principles

Figure 9 shows a full-bridge converter with a diode rectifier, while Figure 10 shows full-bridge converter waveforms under phase-shifted control, which allows a negative drain-to-source current before the MOSFET turns on transients for soft switching. As shown in Figure 10, a phase difference is created between leg 1 MOSFET driving signals (Out1L and Out1H) and leg 2 MOSFET driving signals (Out2L and Out2H), while all four driving signals keep their duty cycle unchanged. When a diagonal pair of MOSFETs turn on, either the input voltage ($+V_{IN}$) or inversed input voltage ($-V_{IN}$) is applied to V_{AB}, which is the time between the energizing

of the series inductor (L_S) and the delivery of energy from the input side (the primary side) to the output side (the secondary side) through the transformer. The phase difference between leg 1 and leg 2 determines the nonzero voltage duration (pulse width) of V_{AB}. A bipolar square wave similar to the V_{AB} waveform is generated at the secondary voltage (V_{SEC}), which will be further rectified by the output diode rectifier to become a unipolar square wave, thus allowing the output inductor to perform "buck" operation for output regulation controlled by the V_{SEC} pulse width.

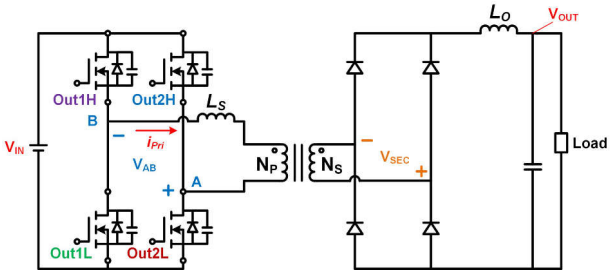

Figure 9. *A PSFB with a full-bridge rectifier.*

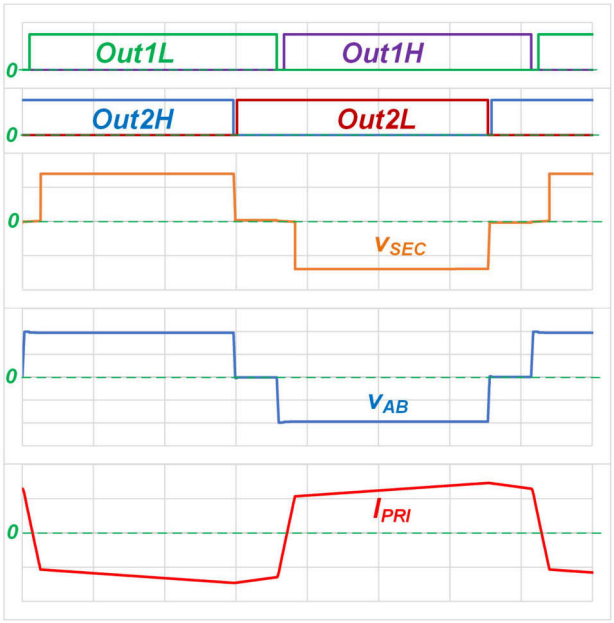

Figure 10. *PSFB waveforms.*

The pulse width of V_{SEC} is smaller than V_{AB} because L_S uses the applied V_{IN} to switch its current polarity, resulting in zero voltage on the transformer winding and thus a smaller V_{SEC} pulse width, which is known as the duty-cycle loss. The larger the L_S inductance, the larger the duty-cycle loss (the difference of pulse widths between V_{AB} and V_{SEC}). Enabling a larger D_{eff} on the secondary side for a wider duty-cycle variation range requires the use of a smaller L_S inductance.

Energy stored in L_S during switching transients is the key to realizing soft switching at the primary-side MOSFETs. A small L_S inductance means less energy stored, which could be insufficient to discharge the MOSFET output capacitor voltage for soft switching, especially at light loads. Thus, you must make a trade-off between soft switching and the D_{eff} ranges in your design.

Because phase-shifted control enables the primary winding current to continuously circulate and freely flow through the primary full-bridge MOSFETs' C_{oss} and body diodes, there may be current lagging on the MOSFETs with inductive impedance at the output of the full-bridge switch nodes and negative current at the MOSFET switching transients, as shown previously in **Figure 8**. Energy stored in L_S is the key to soft switching, but output inductor L_O also affects soft-switching capability.

Let's look at the waveform of MOSFET switching transients. The dashed purple curve in **Figure 11** is the leg 1 high-side MOSFET current. Notice that the leg 1 low-side MOSFET current is identical to the leg 1 high-side MOSFET current but happens at the leg 1 high-side MOSFET turnoff period. You can see that the primary current (I_{PRI}) level at the MOSFET turnon transient is at the L_O current ripple valley point. In other words, leg 1 MOSFET's soft-switching capability will drop if the L_O current ripple is large (that is, if the L_O inductance is smaller). Assuming that the transformer magnetizing inductor current is zero, **Equation 2** expresses the current used to achieve soft switching at the leg 1 MOSFETs as:

$$I_{PRI_{LEG1\_switching\_transient}} = \frac{I_{out,\,avg} - \frac{I_{Lo,\,pp}}{2}}{\frac{N_P}{N_S}} \qquad (2)$$

where $I_{LO,pp}$ is the peak-to-peak current ripple on L_O.

Equation 3 calculates the current used to achieve soft switching at leg 2 MOSFETs as:

$$I_{PRI_{LEG2\_switching\_transient}} = \frac{I_{out,avg} - \frac{I_{Lo,pp}}{2}}{\frac{N_P}{N_S}} \quad (3)$$

Figure 12 highlights the leg 2 low-side MOSFET current with a dashed black line. Notice that the leg 2 high-side MOSFET current is identical to the leg 2 low-side MOSFET current, but happens at the leg 2 low-side MOSFET turnoff period. From **Equation 2** and **Equation 3**, as well as the waveforms in **Figure 11** and **Figure 12**, you can see that it is easier to achieve soft switching for MOSFETs on leg 2 than on leg 1.

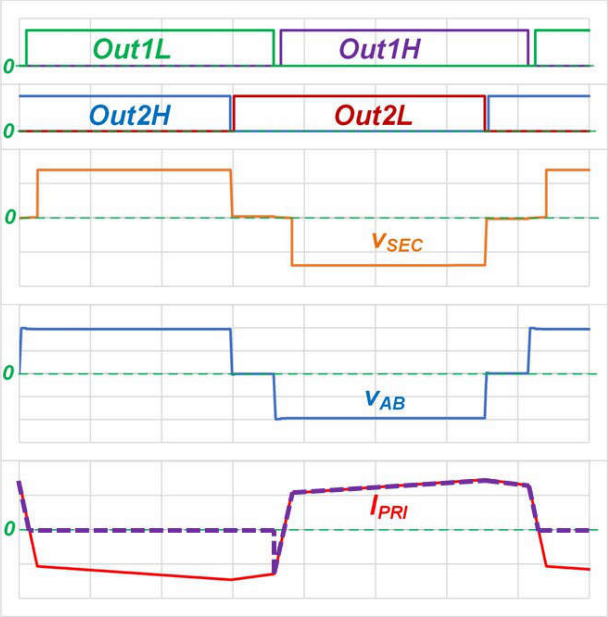

Figure 11. *PSFB waveforms highlighting leg 1 high-side MOSFET current with a dashed purple line.*

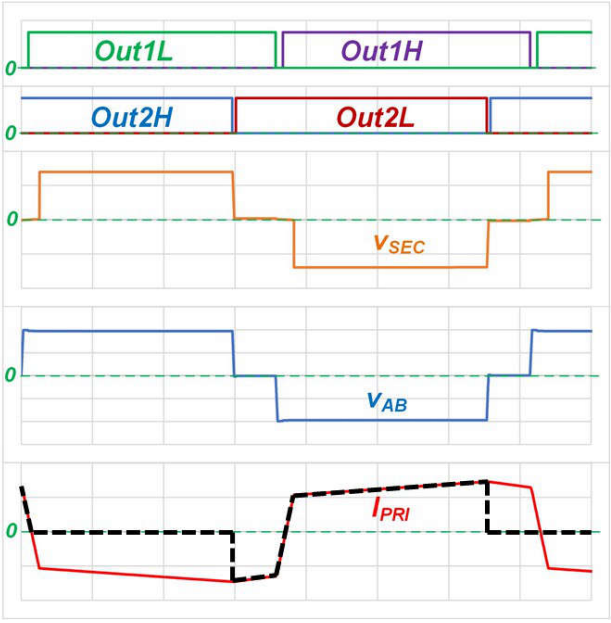

Figure 12. *PSFB waveforms highlighting leg 2 low-side MOSFET current with a dashed black line.*

PSFB Output Rectifiers

The primary function of the rectifier stage in a PSFB is to rectify the bipolar square wave from the transformer winding to a unipolar square wave at the input side of L_O. The type of rectifier that you choose will vary based on different applications and requirements. **Figure 13** through **Figure 15** illustrate three popular rectifiers – the full-bridge rectifier, center-tapped rectifier and current-doubler rectifier – while **Figure 16** and **Figure 17** show rectifier-related waveforms.

With a full-bridge rectifier, a diagonal pair of diodes conducts current to energize L_O when the transformer secondary winding voltage is positive, and the other diagonal pair of diodes conducts current to energize L_O when the transformer secondary winding voltage is negative.

With a center-tapped rectifier, one output diode conducts current to energize L_O when the transformer secondary winding voltage is positive; the other output diode conducts current to energize L_O when the transformer secondary winding voltage is negative.

With a current-doubler rectifier, L_{O1} is only energized through one diode when the transformer secondary winding voltage is positive, and L_{O2} is only energized through the other diode when the transformer secondary winding voltage is negative.

Table 2 lists the differences among these rectifiers. For a PSFB with both full-bridge and center-tapped rectifiers, the L_O operating frequency is double the primary-side MOSFET's switching frequency because of bipolar-to-unipolar waveform conversion. The output inductors of the PSFB with a current-doubler rectifier operate at the same frequency as the primary-side MOSFET's switching frequency. The current-doubler rectifier structure also means that the maximum D_{eff} on the output inductors can only be 50%, while it can be 100% with full-bridge or center-tapped rectifiers.

It is also notable that each rectifier diode has a voltage stress of 2 V_{OUT}/D_{eff} for center-tapped rectifiers and a voltage stress of V_{OUT}/D_{eff} for full-bridge and current-doubler rectifiers. A full-bridge rectifier will have lower rectifier voltage stress compared to a center-tapped rectifier with the same D_{eff} and output voltage (V_{OUT}). Since the maximum D_{eff} of a current-doubler rectifier can only go up to 50%, current-doubler and center-tapped rectifiers will both have higher voltage stress levels than a full-bridge rectifier in efficiency-optimized designs (with D_{eff} closed to its maximum) with the same V_{OUT}.

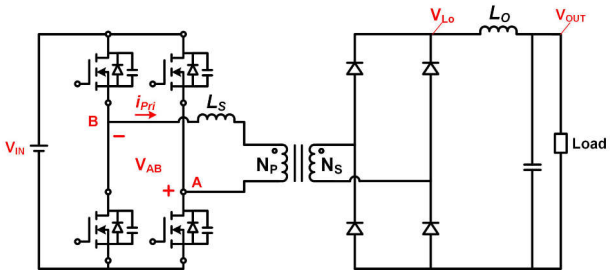

Figure 13. *A PSFB with a full-bridge rectifier.*

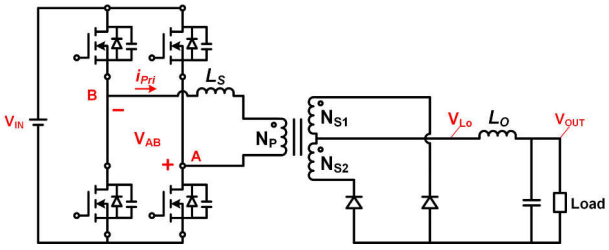

Figure 14. *A PSFB with a center-tapped rectifier.*

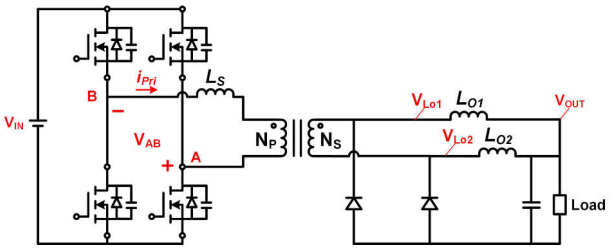

Figure 15. *A PSFB with a current-doubler rectifier.*

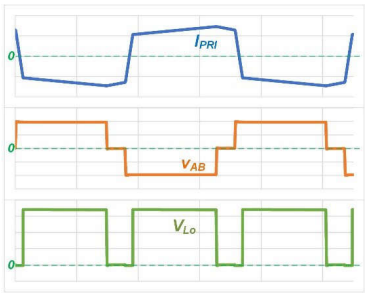

Figure 16. *Waveforms of a PSFB.*

Note

Waveforms with either a full-bridge rectifier or a center-tapped rectifier.

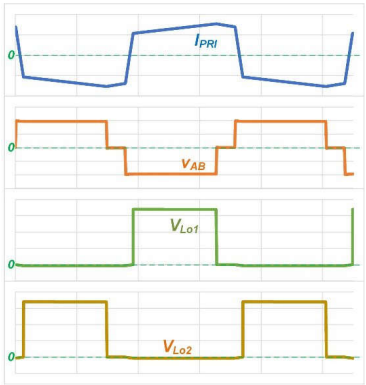

Figure 17. *Waveforms of a PSFB with either a full-bridge rectifier or a center-tapped rectifier.*

Rectifier type	Inductor operating frequency	Allowed D_{eff} range	Number of secondary windings	Number of rectifier components	Number of output inductors	Characteristics
Full bridge	Twice the primary switching frequency	0-100%	1	4	1	Better transformer utilization rate, good for high quiescent output voltage (V_o)
Center tapped	Twice the primary switching frequency	0-100%	2	2	1	Lowest component count, lower transformer utilization rate
Current doubler	The primary switching frequency	**0-50%**	1	2	**2**	Better transformer utilization rate, half I_{LO}

Table 2. *Primary characteristics of PSFB output rectifiers.*

Clamping Options for a PSFB

A PSFB can achieve soft switching on its primary-side switches and have a clean FET drain-to-source voltage (V_{DS}) waveform without much voltage ringing. However, the PSFB output rectifier parasitic capacitance will resonate with the inductance in series with the transformer windings and lead to high rectifier voltage stress.

Consider the PSFB with a full-bridge synchronous rectifier in **Figure 18**. The synchronous rectifier V_{DS} voltage will have large ringing, with the FET output capacitance modeled as shown in **Figure 19**. The peak value of the ringing could be as high as $2V_{IN} \times N_S/N_P$. In order to reduce the rectifier voltage stress and thus use lower drain-to-source on-resistance ($R_{DS(on)}$) FETs for better efficiency, you might need to clamp the rectifier voltage stress. One option is to apply a passive clamp circuit to absorb partial energy in the voltage ringing. **Figure 20** shows a passive clamp option applied to a PSFB. **Figure 21** shows how the addition of a resistor-capacitor diode at the output stage greatly reduces the rectifier voltage stress. The capacitance of the clamping capacitor (C_{cl}) needs to be large enough to be treated as an ideal voltage source in order to effectively clamp the rectifier voltage stress. C_{cl} is charged by the clamping diode and dissipates its energy on R_{cl}. **Equation 4** calculates the clamping resistor (R_{cl}) resistance required to clamp the rectifier voltage at the targeted clamp voltage level (V_{CP}):

$$R_{cl} = \frac{(V_{CP} - V_{OUT}) \times (V_{CP} - V_d)}{C_{cl} \times V_{CP} \times (2V_d - V_{CP}) \times f_{SW}} \quad (4)$$

where $V_d = V_{IN} \times N_S/N_P$ and f_{SW} is the PSFB switching frequency.

Equation 5 calculates the power dissipation on the clamping resistor as:

$$P_{R_{cl}} = \frac{(V_{CP} - V_{OUT})^2}{R_{cl}} \quad (5)$$

As **Equation 4** and **Equation 5** illustrate, a lower V_{CP} requires lower R_{cl} and higher power dissipation on R_{cl}.

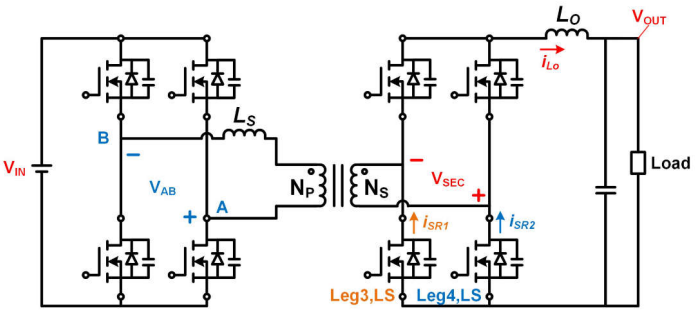

Figure 18. *A PSFB with a synchronous rectifier.*

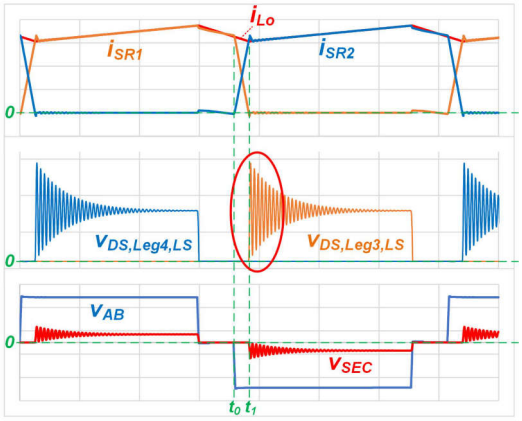

Figure 19. *Waveforms of a PSFB without voltage clamping on the output rectifier.*

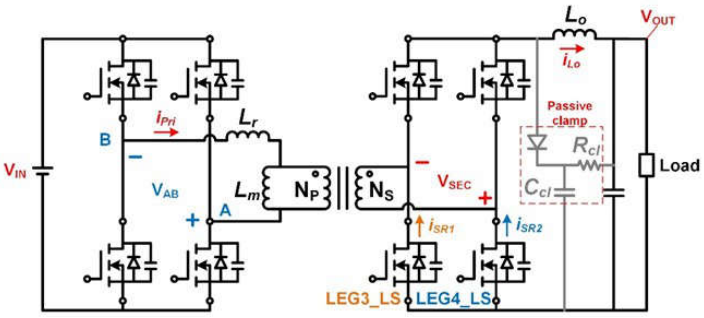

Figure 20. *A PSFB with a passive clamp.*

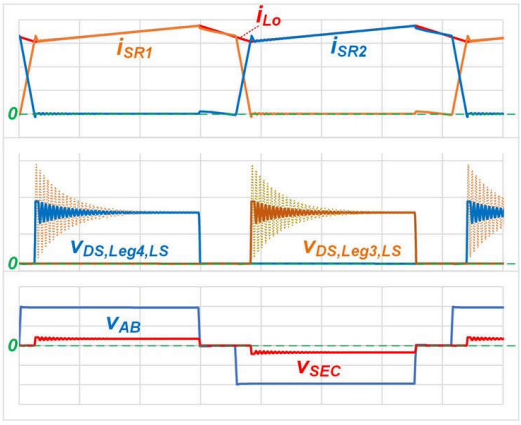

Figure 21. *Waveforms (with solid lines) of a PSFB with a passive clamp circuit.*

A PSFB relies on energy stored in the inductor in series with the transformer winding to achieve soft switching. But the inductor will resonate with the rectifier parasitic capacitors, resulting in high rectifier voltage stress. If you can reduce the inductance of the transformer series inductor, you can reduce the rectifier voltage stress.

A primary clamp, shown in **Figure 22**, can enable the use of a smaller series inductor by adding two diodes, with the transformer series inductor placed between the half-bridge FET leg and the clamping diodes. By doing so, the only transformer series inductor will be the transformer leakage inductor.

Figure 23 shows waveforms of a PSFB both with and without a primary clamp. L_S is set to 3.5 µH and the leakage inductance (L_{lk}) is set to 0.5 µH. With the diode clamp at the primary side, it is possible to recycle the energy in L_S and keep it at the primary side. The output rectifier parasitic capacitor will only resonate with L_{lk}, reducing output rectifier voltage stress significantly. Because you need the discrete inductor L_S in a PSFB with a primary clamp to maintain soft switching with a small L_{lk}, the power density might be lower than a PSFB with another clamping method.

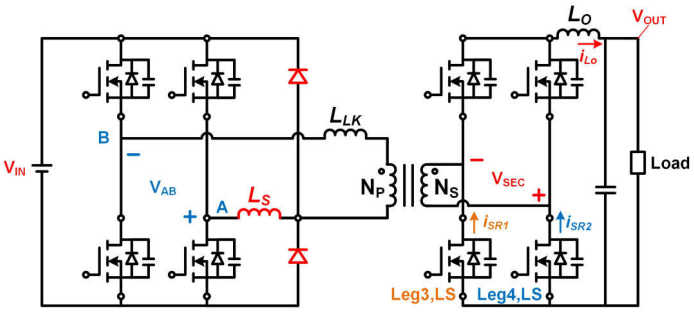

Figure 22. *A PSFB with a primary clamp.*

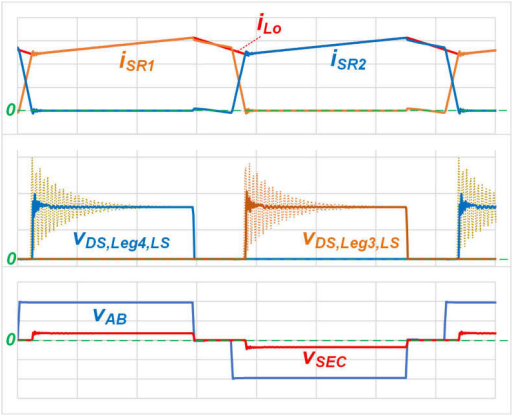

Figure 23. *Waveforms of a PSFB both with (solid lines) and without (dashed lines) a primary clamp circuit.*

Instead of burning power on a clamp resistor such as a passive clamp or adding a discrete inductor such as a primary clamp, using the active clamp shown in **Figure 24** could help optimize both size and efficiency. An active clamp leg (ACL) formed by a capacitor (C_{CL}) and a MOSFET (Q_{CL}) is inserted before the output inductor. When the output winding voltage becomes nonzero, energy will transfer from the primary winding to the secondary winding to energize the output inductor and also conduct current through the Q_{CL} body diode to charge C_{CL}, even if Q_{CL} is not turned on. Turning on Q_{CL} after its body has already conducted current will ensure zero voltage switching (ZVS) on Q_{CL}. It is important to turn on Q_{CL} before the current polarity change in order to allow the completion of the current-second balance (or charge balance) on C_{CL} at the beginning of $D_{eff}T_S$.

Figure 25 shows that there is a nonmonotonic current on the synchronous rectifier current as well as the transformer winding current, which could pose challenges for peak current-mode control, since peak current-mode control generally requires a monotonic current rise on transformer current during the effective duty-cycle period. Q_{CL} only needs to be turned on long enough for the active clamp current-second balance to work as intended – to clamp the output rectifier voltage to the C_{CL} voltage (V_{CL}). Q_{CL} doesn't need to conduct throughout the full $D_{eff}T_S$, but for a relatively short period of time instead.

Therefore, we propose setting Q_{CL} to have a fixed-on time ($D_{ACL}T_S$ = constant) while keeping $D_{eff}T_S$ always greater than the duration where the current-second balance is completed ($D_{CSB}T_S$) under whole operational voltage and load ranges. Since $D_{eff}T_S$ is larger than $D_{CSB}T_S$, peak current detection will always occur when the transformer current rises monotonically. The PSFB is generally designed to have a larger D_{eff} at mid to heavy loads, where $D_{eff} >> D_{CSB}$ is expected. At light loads, the converter usually operates under discontinuous conduction mode, where D_{eff} will be smaller than D_{eff} under continuous conduction mode at the same input/output voltage condition.

In order to keep $D_{eff}T_S$ greater than $D_{CSB}T_S$ even at light loads, you can implement frequency reduction control or burst operation. It is important to turn on Q_{CL} only after the duty-cycle loss period has ended; otherwise, the energy stored in C_{CL} will dump back to the primary side, overstress the synchronous rectifier, and potentially damage the components. C_{CL} needs to be large enough to be treated as an ideal voltage source to effectively reduce the synchronous rectifier voltage stress. Therefore, you must ensure that C_{CL} selection meets the inequality expressed by **Equation 6**:

$$T_S \ll 2\pi\sqrt{\left(\frac{N_S}{N_P}\right)^2 L_S C_{CL}} \quad (6)$$

Assuming zero voltage ripple on C_{CL}, it is possible to clamp the rectifier voltage to $V_{IN}N_S/N_P$, which is half the voltage stress without any clamp circuit. The active clamp doesn't dissipate the ringing energy on the power resistor but circulates the energy in the LC resonant tank as a lossless snubber. Therefore, you can expect higher converter efficiency on a PSFB with an active clamp than on a PSFB with a passive clamp in an identical specification.

The synchronous rectifier C_{oss} will control the peak current on the ACL. Selecting a low C_{oss} synchronous rectifier FET will mean a lower ACL root-mean-square (RMS) current and thus help improve converter efficiency.

Here are some design guidelines when designing a PSFB with an active clamp:

- Q_{CL} must turn on only after a duty-cycle loss duration to avoid C_{CL} energy backflow to the primary side.
- Q_{CL} must turn on while the body diode is still conducting current for ZVS.
- A longer Q_{CL} on-time will reduce V_{CL} as well as synchronous rectifier voltage stress, but the Q_{CL} RMS current will increase.

- A lower synchronous rectifier C_{oss} not only helps reduce ACL RMS current, but also helps reduce synchronous rectifier voltage stress.

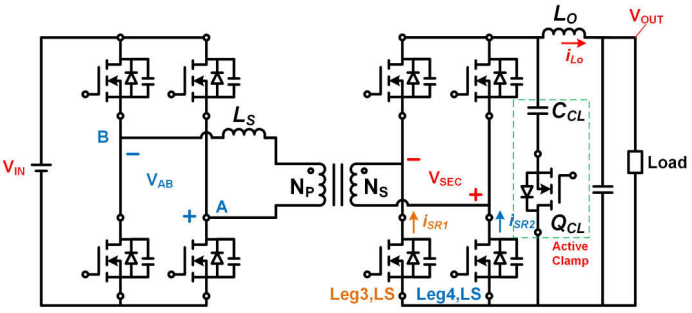

Figure 24. *A PSFB with an active clamp.*

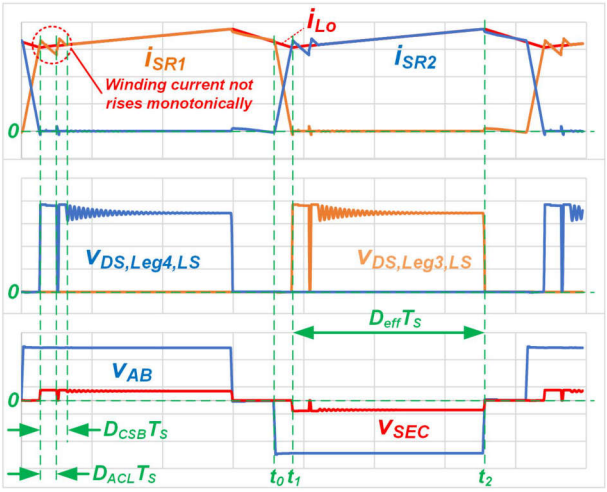

Figure 25. *Waveforms of a PSFB with an active clamp.*

PSFB Control

This section introduces some of the nuances concerning the control of a PSFB. **Figure 26** is a high-level block diagram of the control logic needed to implement a PSFB, where OUT1H and OUT1L are the gate logic for one half bridge of the primary FETs and OUT2H and OUT2L are the gate logic of the other half bridge of the primary FETs. A clock set to the intended switching frequency directly controls the OUT1H and OUT1L PWM pair. The OUT2H and OUT2L are controlled by a combination of:

- A ramp signal consisting of a resistor, capacitor and a fixed reference voltage, V_{RAMP_REF}.
- An error amplifier that samples the output voltage through a resistor divider with a compensation network.
- A comparator that compares the output of the error amplifier and the ramp signal voltage.
- A T flip-flop that sets the state of OUT2H and OUT2L based on the comparator output. The T flip-flop is rising edge-triggered.

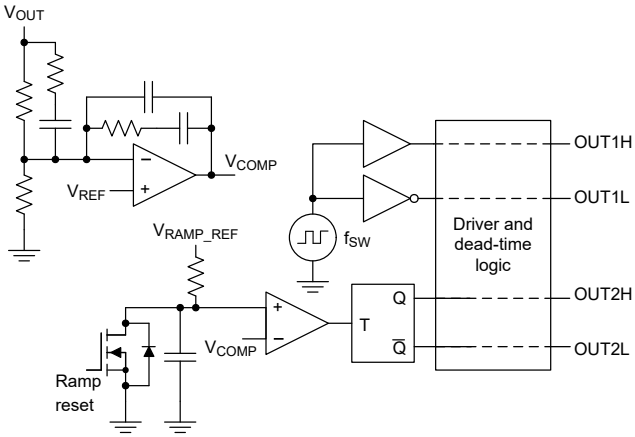

Figure 26. *PSFB control logic.*

Figure 27 illustrates the gate-logic waveforms of the circuit shown in **Figure 26**. At the beginning of a new switching cycle, the ramp signal resets to 0 V and the diagonal pair of primary FETs, OUT1H and OUT2L, turn on. When the ramp signal, V_{RAMP}, becomes larger than the error amplifier output voltage, V_{COMP}, the T flip-flop toggles, changing the state of OUT2H and OUT2L. At the halfway point of the switching period, the state of OUT1H and OUT1L changes and the ramp voltage resets. The other diagonal pair of primary FETs, OUT1L and OUT2H, are now on. When the ramp signal exceeds the error amplifier output voltage, the T flip-flop toggles again, changing the state of OUT2H and OUT2L.

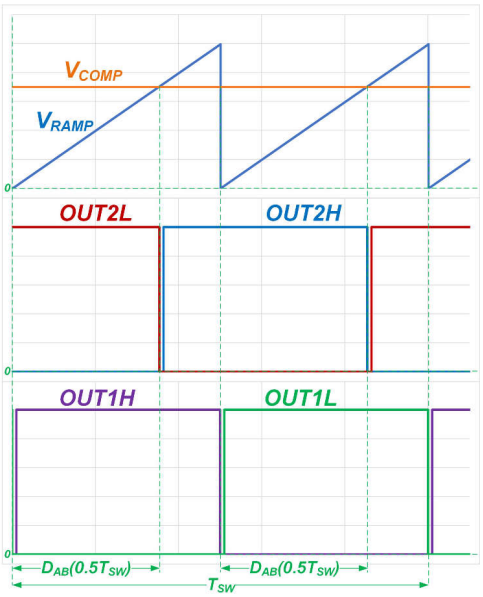

Figure 27. *PSFB control logic waveforms.*

The control logic we've just described is known as voltage-mode control. **Figure 28** shows a slight variation of this control logic, which uses V_{IN} or a voltage proportional to V_{IN} instead of a fixed reference voltage to generate the ramp signal. The advantage of this method is that the control logic instantly reflects changes in V_{IN}, as the transient voltage (dV/dt) of the ramp immediately changes with V_{IN}. This minimizes deviations of V_{OUT} caused by changes in V_{IN}.

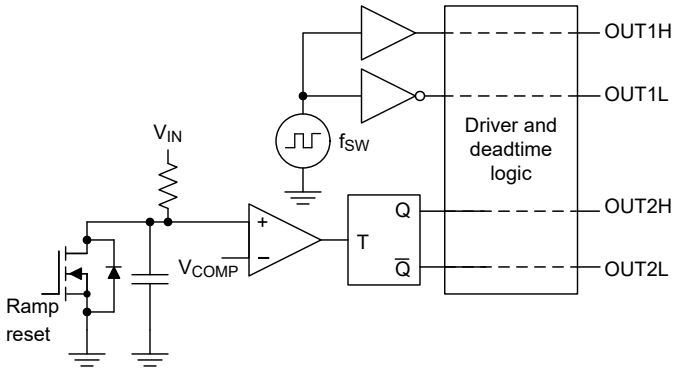

Figure 28. *Voltage-mode control with feedforward.*

Figure 29 shows another variation of the control logic known as peak current-mode control. This method replaces the ramp signal with sampled current information, I_{CS}, from the power stage.

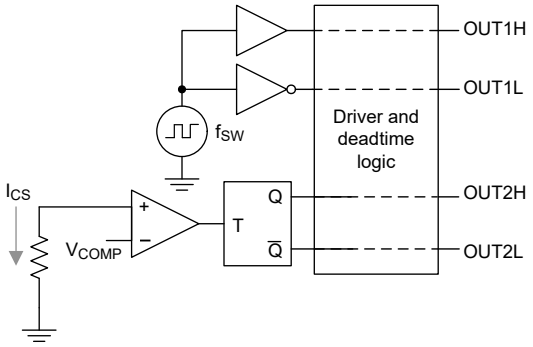

Figure 29. *Peak current-mode control.*

The decision to use voltage-mode control or peak current-mode control has ramifications for the design of the power stage of the PSFB. For voltage-mode control, you would need to place a DC blocking capacitor in series with the transformer primary winding, as shown in **Figure 30**, in order to avoid the transformer saturation issue caused by the winding current imbalance. Because all of the transformer primary winding current flows through the DC blocking capacitor, you will need a sufficient current rating capacitor or a combination of capacitors that satisfy the required current rating. The voltage stress of the rectifiers on the secondary side increases when applying the DC blocking capacitor. That is because the DC blocking capacitor voltage ripple makes the transformer primary winding voltage amplitude greater than V_{IN} when a diagonal pair of primary MOSFETs turns on. Therefore, you must make a trade-off between the size and capacitance of the DC blocking capacitor and the voltage stress.

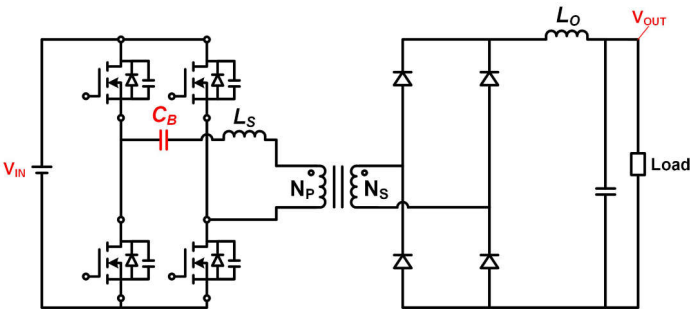

Figure 30. *A PSFB with a DC blocking capacitor.*

One of the benefits of current-mode control is that the DC blocking capacitor is not required, as the control loop directly samples and regulates the peak current of the transformer. **Figure 31** circles three locations where it is possible to implement power-stage current sampling.

Location No. 1 places a current-sensing element such as a current-sense transformer in series with the PSFB transformer. One of the benefits of this location is that you can automatically reset the current-sense transformer core because of the bidirectional current flow of the PSFB transformer. One of the disadvantages of this location is that the current-sense signal from the transformer only contains AC information but not DC information. Items such as delay mismatches in the power stage or common-mode noise coupling into the current-sense signal can bias the PSFB transformer current to one side, potentially requiring a larger margin on the transformer design to avoid saturation.

Location No. 2 places the current sampling between the input capacitor and the full bridge on the primary. You can place a transformer between the input capacitor and the full bridge or in the return path from the full bridge going back to the input capacitor. The benefit of this location is that the current-sense signal of the transformer contains both AC and DC information and avoids the disadvantages of location No. 1. The drawback of location No. 2 is an increase in the parasitic inductance within the primary-side power-stage loop. It is important to manage the voltage stress on the primary FETs caused by ringing coming from higher parasitic loop inductance. Another challenge of this location is the need to reset the transformer core twice every switching cycle. This reset occurs when both high-side or both low-side primary FETs are on. The transformer core reset becomes even more challenging for designs requiring a high duty cycle or high-frequency designs where the amount of time to complete the reset is smaller. It is also possible to use a shunt resistor plus a current sense amplifier as a current-sensing element in the return path from the full bridge going back to the input capacitor. This avoids any transformer reset challenges, with the trade-off of power dissipation in the shunt resistor.

Location No. 3 is on the secondary side in the return path of the output inductor current going back to the rectifiers. Designers often use a current-sense resistor and current-sense amplifier for this location. Unlike the other two locations, the current sampling is located on the converter's secondary side, which can simplify the implementation if the PSFB controller is also located on the secondary side, since there is no need to cross the isolation barrier. Among the three locations, when applying active clamping, location No. 3 is the only location that doesn't have distorted current during the current ramping period.

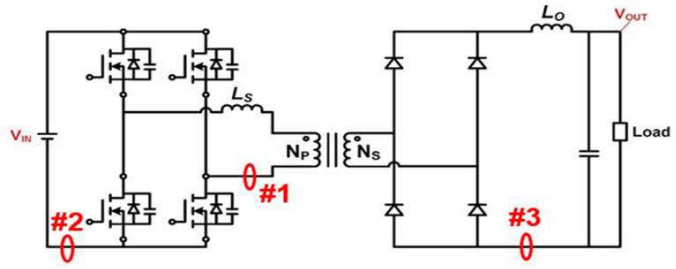

Figure 31. *A PSFB with current-mode control.*

Figure 32 compares the plant transfer function of the voltage mode-controlled PSFB model presented by Christophe Basso in "Transfer Functions of Switching Converters" and the plant transfer function of the peak current mode-controlled PSFB model presented by Shi-Song Wang in "Small-Signal Modeling of Phase-Shift Full-Bridge Converter with Peak Current Mode Control" for a 3-kW, 400-V_{IN} to 12-V_{OUT} PSFB converter operating at 100 kHz. The PSFB is a buck-derived topology, and while you may expect similarities between the voltage mode-controlled buck and the voltage mode-controlled PSFB, the impact of duty-cycle loss caused by L_S results in a damping effect, such that there is an absence of peaking in the AC response of the voltage mode-controlled PSFB. The voltage mode-controlled model presents two real poles in its plant transfer function, while the peak current mode-controlled model presents

one real pole. The softer rolloff of the gain in peak current-mode control suggests that it has an advantage because it achieves a higher loop bandwidth, which is appealing for applications where load transient response is a concern.

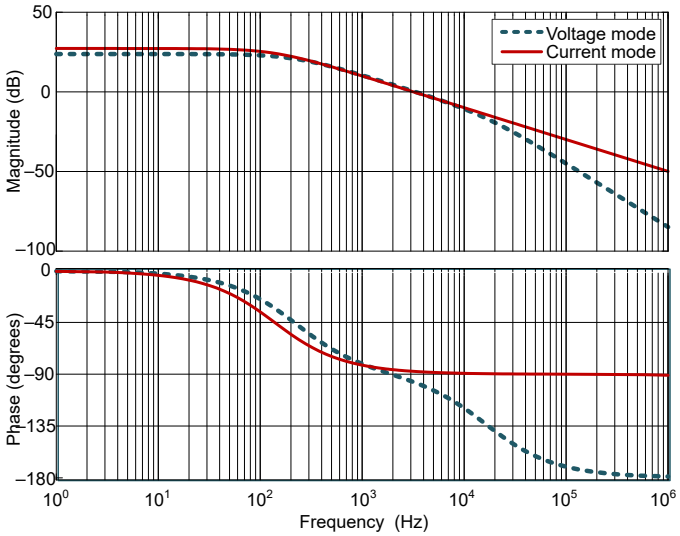

Figure 32. *Comparing voltage-mode control vs. peak current-mode control.*

Synchronous Rectifier Modes of Operation

Synchronous rectifier operation modes in a PSFB converter can be different from other isolated topologies such as an LLC-SRC. A synchronous rectifier in an LLC-SRC works like an ideal diode. Detecting the synchronous rectifier FET voltage or current reveals whether current is conducting through the body diode of the FET, so that you know whether to turn on the synchronous rectifier FET. When synchronous rectifier current is lower than a certain level, turn off the synchronous rectifier FET.

As PSFB rectifier stage (shown in **Figure 33**) operates like a buck converter. For example, when V_{SEC} is positive, L_O is energized through the leg 4 high-side switch (controlled by the Out4H signal) and current returning to the transformer through the leg 3 low-side switch (controlled by the Out3L signal). When the transformer winding voltage is zero, I_{LO} current continuously flows through the leg 4 low-side switch (controlled by the Out4L signal) and current returns to L_O through the leg 3 high-side switch (controlled by Out3H). This is the freewheeling period, during which the inductor current will continue to flow through the body diodes of the synchronous rectifier FETs, even you don't turn them on. When the current during the freewheeling period is high, you must turn on all four of the synchronous rectifier FETs in the full-bridge rectifier to allow channel conduction instead of body diode conduction to lower the conduction losses. In general, there are three modes of operations of the synchronous rectifier in a PSFB, as shown in **Figure 34** through **Figure 36**. When the load current is very low, it is acceptable to keep all synchronous rectifier FETs turned off (mode 0) to lower the switching and driving losses. When the load current is a little bit higher while the PSFB is still in discontinuous conduction mode, you can start to turn synchronous rectifier FETs on during the L_O energizing period (mode 1). When the load current goes even higher, the PSFB operates in continuous conduction mode, turning all synchronous rectifier FETs on during the L_O de-energizing period (mode 2) to help lower the conduction losses. The ability to turn all four synchronous rectifier FETs of the full-bridge rectifier on during the freewheeling period is unique to a PSFB.

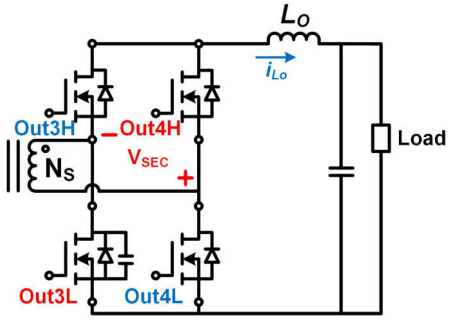

Figure 33. *PSFB output stage with a synchronous rectifier.*

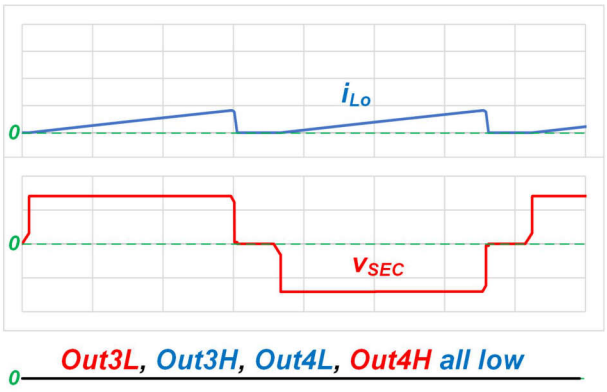

Figure 34. *Synchronous rectifier modes of operation: mode 0 – all synchronous rectifier FETs are turned off at light loads.*

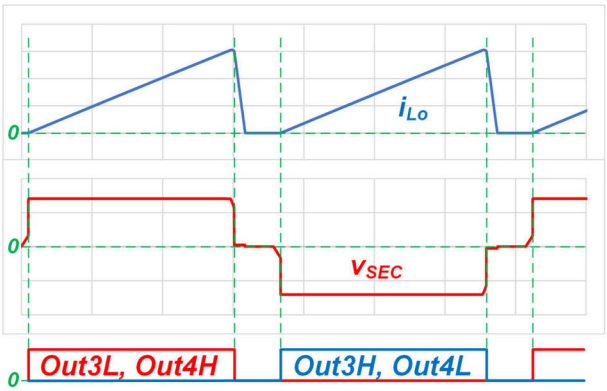

Figure 35. *Synchronous rectifier modes of operation: mode 1 – only turn on corresponding synchronous rectifier FETs when L_O is energizing.*

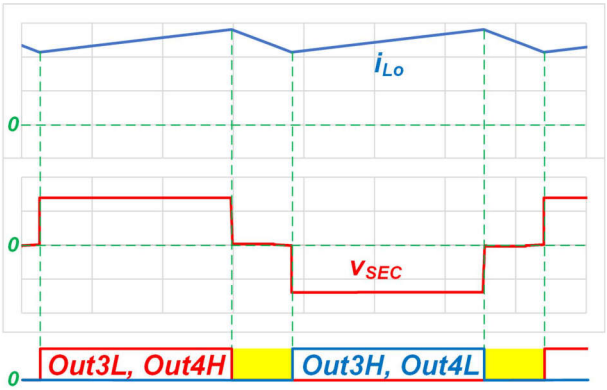

Figure 36. *Synchronous rectifier modes of operation: mode 2 – turn on all synchronous rectifier FETs when L_O is de-energizing.*

Light-Load Management Options

At light loads, it may be necessary to use a specialized control mode in order to maintain the output voltage within regulation or to improve the efficiency of the PSFB converter. One such method is to directly reduce the switching frequency of the converter and extend the periods of OUT1H/OUT2H and OUT1L/OUT2L overlap, as shown in **Figure 37**. This method enables the PSFB to achieve lower D_{eff} while maintaining a minimum overlap time for each OUT1H/OUT2L and OUT1L/OUT2H diagonal pair. Given the longer on-time of each primary gate signal, we do not recommend this method when using a gate-drive transformer on the primary side, as it becomes challenging to avoid saturating it.

Figure 38 illustrates a second light-load management scheme. In this method, the PSFB converter stops switching entirely if the output of the error amplifier, V_{COMP}, falls below a preset value, $V_{burst\_threshold}$. When V_{COMP} becomes larger than $V_{burst\_threshold}$, the PSFB resumes switching. One of the benefits of this hysteretic burst-mode approach compared to frequency-reduction mode is lower CPU utilization, since the controller does not need to compute the required switching frequency. Hysteretic burst mode also has a higher loop bandwidth at light loads compared to frequency-reduction mode. The primary disadvantage of this approach is a higher output-voltage ripple.

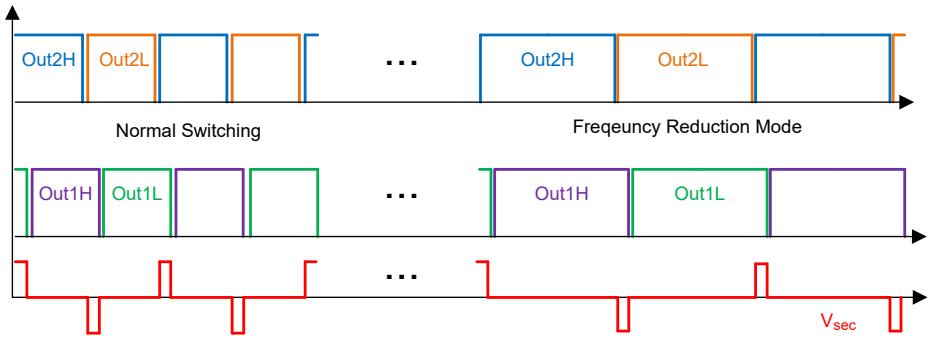

Figure 37. *PSFB switching pattern with frequency-reduction mode.*

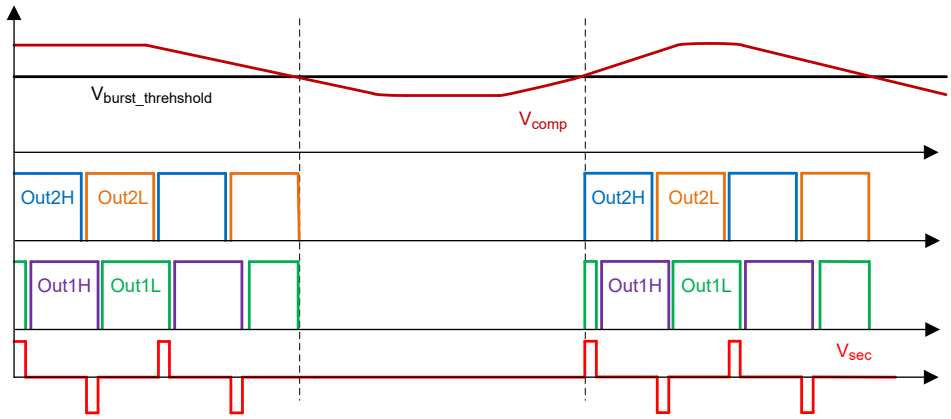

Figure 38. *PSFB switching pattern with hysteretic burst mode.*

PSFB Design Example

To verify performance, we built a 54-V, 3-kW PSFB with an active clamp reference design targeting the M-CRPS specification. **Figure 39** and **Figure 40** show the block diagram and board photo of this reference design, respectively. The reference design uses the TMDSCNCD280039C C2000™ microcontroller for PSFB control, gallium nitride FETs for efficiency optimization, and a current transformer on the primary winding for peak current-mode control current sensing. The total power-stage dimensions are 100 mm by 65 mm by 40 mm. **Figure 41** shows steady-state waveforms at a 3-kW load. The active clamp MOSFET is programmed to turn on for only 300 nS with a 140-kHz PSFB switching frequency, therefore limiting the nonmonotonic I_{PRI} duration to less than 1 µS and allowing a wide D_{eff} range. The transformer secondary winding voltage (V_{SEC}) peak represents synchronous rectifier FET voltage stress. **Figure 41** also shows the 80-V voltage stress on the synchronous rectifier FETs with a 54-V output, enabling us to use 100-V rated synchronous rectifier FETs. **Figure 42** shows a 50% load transient with a 1-A/µS current-changing slew rate. This reference design demonstrates much better performance than M-CRPS limits.

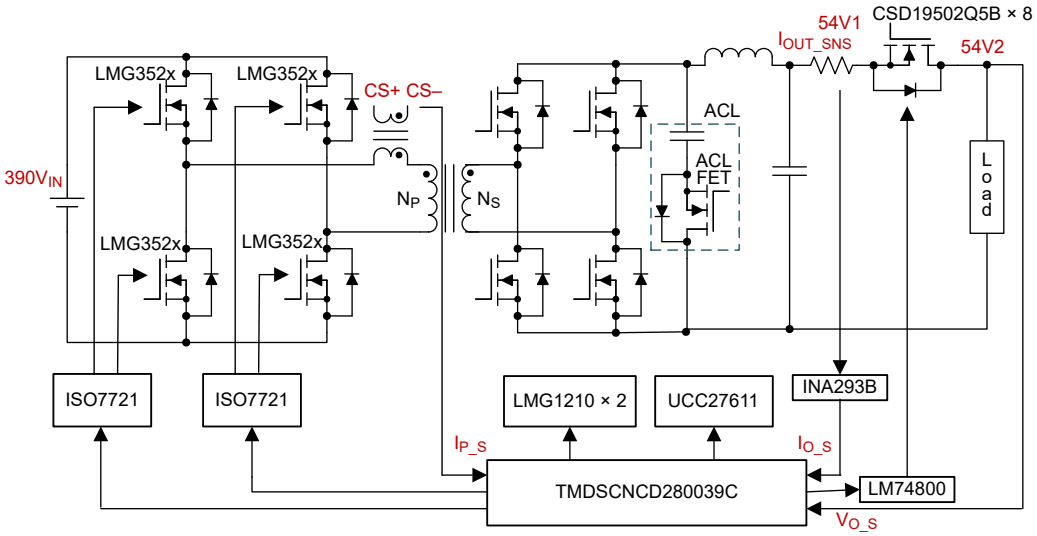

Figure 39. *54-V, 3.6-kW PSFB with active clamp reference design.*

Figure 40. *54-V, 3.6-kW PSFB reference design.*

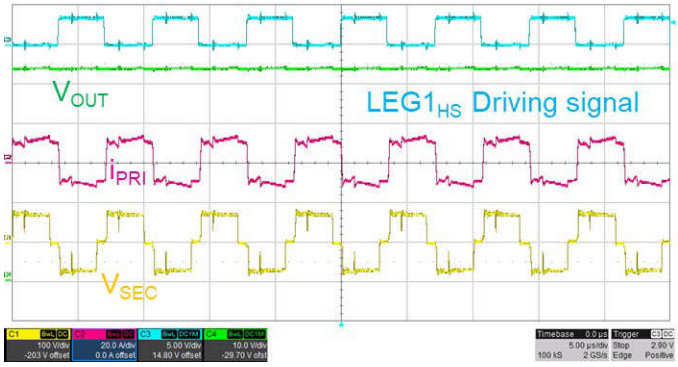

Figure 41. *Steady-state waveforms of the PSFB reference design at a 3-kW load.*

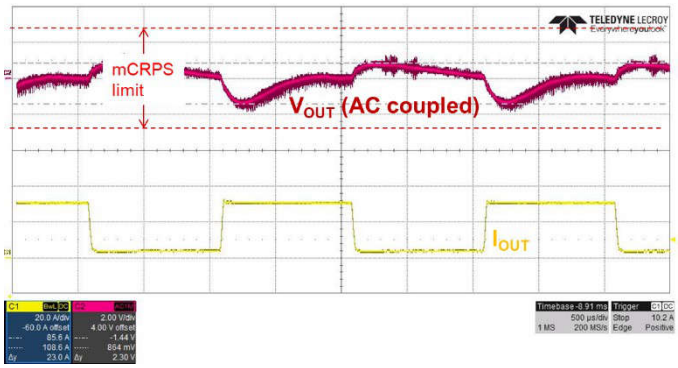

Figure 42. *3-A to 31-A (50%) load transient based on the M-CRPS specification.*

Conclusions

A PSFB is a good candidate for applications that require a wide input/output voltage range and a fast load transient response. In this paper, we discussed PSFB fundamentals including operational principles, types of rectifiers, rectifier clamping options, modes of controls, synchronous rectifier operational modes, control modes and light-load management schemes.

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