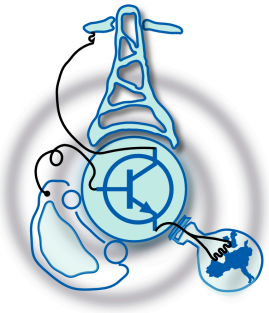
Implementation of a Phase Shifted Full bridge DC-DC ZVS converter with peak current mode control

by

Assel Zhaksylyk



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems

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Abstract

The demand for robust and efficient power supplies is driving the research of various Switched-Mode Power Supply (SMPS) architectures and enhanced control strategies. In this thesis, comparative analysis of Full-Bridge LLC and Phase-Shifted Full-Bridge converters, center-tapped and bridge rectifiers, synchronous and passive rectifiers has been performed. Zero-voltage switching resonant considerations for the Phase-Shifted Full-Bridge have been studied. A 600W Phase-Shifted Full-Bridge DC-DC ZVS converter using peak current mode control has been designed and implemented. Aspects of the hardware implementation of an isolated SMPS, such as electromagnetic interference, high voltage isolation, efficiency, effects of parasitic components are studied and discussed. The theoretical design of a converter is compared with and validated by simulation and experimental results. The converter demonstrated 87-90% efficiency, and relatively stable operation at 1.3kHz bandwidth with good phase and gain margin.

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Chapter 1

Introduction

Modern electronic devices depend upon a high quality, reliable and efficient power supplies. This project, in particular, was developed upon the request for a 600W, 300V power supply with very stringent ripple specifications, to be connected after a power factor correction (PFC) rectifier stage, that provides a 390V output. Technical specifications of the required power converter will be given in the following chapters. However, the application of this converter and some details cannot be shared due to non-disclosure agreement. Therefore, this converter will be considered a power supply for generic and varying load with maximum value of 600W with specifications as described in Chapter 5. Moreover, even though the converter is 600W, the project needed to be easily adjustable and scalable for future prototypes, and potentially used up to 3kW just by replacing the components without changing the printed circuit board (PCB). This converter was designed, prototyped and tested at the SP Control Technologies (SPC) laboratory in Madrid, Spain. SP control technologies is a power electronics company with a special focus on magnetic elements. Magnetic components used in this project were designed using Frenetic AI software (Property of SPC).

1.1 Introduction to Power supplies

There are three broad types of power supplies: unregulated, linear regulated, and switched-mode power supply (SMPS). An unregulated power supply is the most primitive type. By their nature, unregulated power supplies do not produce a constant voltage as regulated power supplies do. The output voltage of the unregulated power supply may change based on the output current, and also exhibits more ripple. Moreover, the output voltage will also change if the input voltage is varying. Linear regulated power supply circuit is usually an unregulated power supply followed by a transistor circuit. This type of power supply allows having a somewhat controlled output voltage. However, it can only decrease the unregulated input voltage, and the excess voltage will be dissipated in the form of heat. So, the efficiency of the linear regulated power supply will be proportional to the ratio between output and input voltages. Moreover, the switch in linear power supplies operates in the active region, which results in very low efficiency. Therefore, linear voltage regulators are not used in high power applications. According to [2], by using isolated Switched-mode power

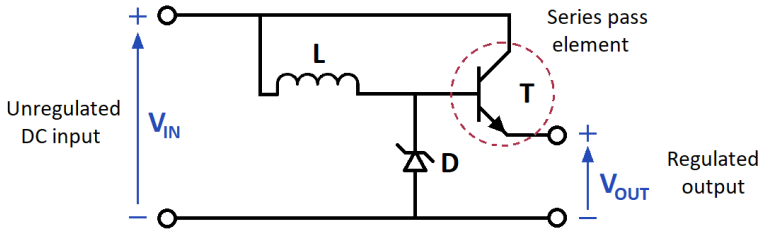

Figure 1-1: Schematic of a linear voltage regulator

supplies (SMPS) with wide-bandgap (WBG) semiconductor devices, an efficiency of 99% can be achieved. Therefore, only SMPS will be studied in the following parts of this document.

1.1.1 Switched-mode Power supplies

Switched-mode power supplies convert unregulated DC or AC voltage to a controlled DC voltage. The power from the AC mains is first rectified and filtered. Then this

unregulated DC voltage is supplied to a DC-DC converter. This converter needs to provide DC output of the desired level with minimal AC ripple, despite the changes in the input voltage or the load. Moreover, most of the systems nowadays require isolation between the source and the load, which is essential for safety and noise issues. In SMPS it is achieved by using an intermediate AC stage and a transformer. However, to avoid bulky magnetic components, the switching frequency of the converter is usually in the range of hundreds of kHz. Also, the transformer is used to scale the voltage up or down to achieve the optimal point of operation. As the name

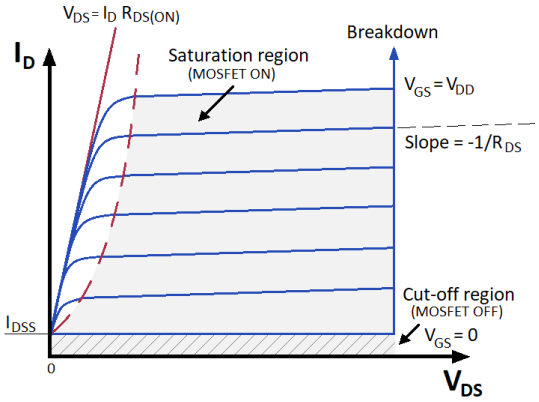

Figure 1-2: Regions of the FET transistor on the IV

implies the "Switched-Mode Power Supplies" use number of switches that turn-on and turn-off at a high frequency. When the switch is conducting (on-state), it is in the saturation region (Figure 1-2): current flows through the drain and source, but the voltage drop is very small. During the off-stage, the switch is in the cut-off region with almost no current flowing between its terminals. This way, most of the power loss on the component occurs during the switching, as shown in Figure 1-3 (a). That means with higher switching frequency more losses occur. Therefore, there should be a tradeoff between the switching losses and the size of magnetic components when choosing the frequency. In Figure 1-3 power loss is defined by the gray area. If magnitudes of current and voltage are high during the switching transient, "hard switching" is observed. During hard switching, instantaneous losses and stress on the semiconductor devices are high. Moreover, hard switching creates electromagnetic interference (EMI) problems. The alternative of the hard switching is called

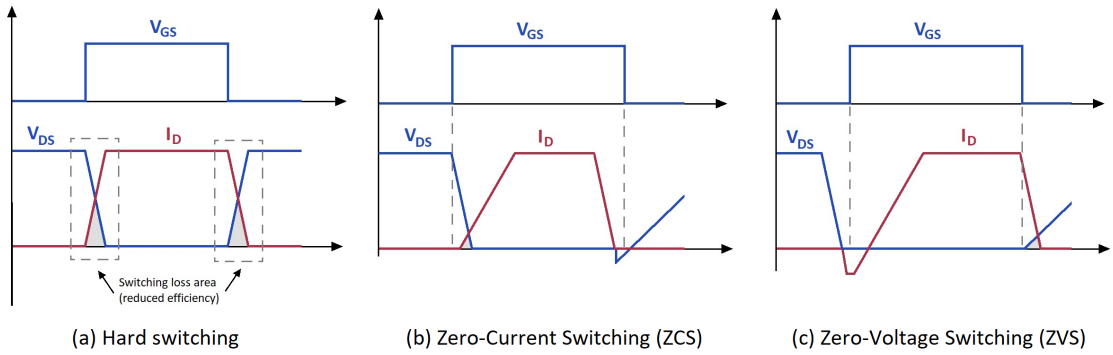

Figure 1-3: Hard switching

soft switching. The soft switching is observed if the current or voltage is zero (Figure 1-3 (b-c)) or close to zero during the transient. This switching method is more challenging to implement because the switch timing must be controlled to match current and voltage waveforms.

1.1.2 Soft-switching Power Supplies

Figure 1-4 (a) demonstrates zero current switching (ZCS) of the power FET. However, this is also valid for insulated-gate bipolar transistors (IGBT) and gate turn-off thyristors (GTO). Due to the series inductor, when FET is turning on, the drain-to-source voltage falls to almost zero before current flows through its terminals. Therefore, turn-on losses on the device are very low. However, the energy stored in a drain-to-source capacitance will be dissipated in the form of heat. At turn off, the voltage between the drain and source terminals decreases and reverses, as shown in Figure 1-4 (a). The reversed voltage causes the current to flow in the opposite direction and gates the device off. So, when voltage is reapplied, the device is in the off-state, and ideally, no turn-off losses appear. To conclude, the ZCS is able to decrease the turn-on losses and eliminate turn-off losses.

Another example of soft switching is zero-voltage switching (ZVS). In this case, due to the capacitive element in parallel with the power FET device (separate capacitor or the parasitic drain-to-source capacitance of the device) turn off losses are decreased as shown in Figure 1-4 (b). At turn on, the drain-to-source voltage is de-

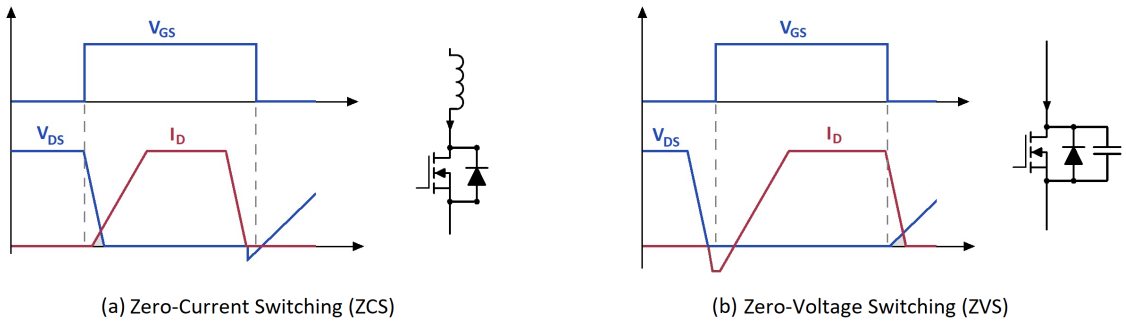

Figure 1-4: Soft switching circuit transients

creased through the external resonant circuit. So, when the device is gated on, the voltage is zero, and very low turn on losses occur. Moreover, unlike ZCS, during turn on, the energy of the parallel capacitance is not dissipated in the device but returned to the circuit through resonant action. Since the capacitive turn on losses occur at every cycle for ZCS circuits, they are proportional to the switching frequency. Therefore, for higher frequency ($\geq 1MHz$) applications, the ZVS topologies are preferred. Zero voltage switching applied to the selected converter topology will be discussed in detail in the following chapters.

1.2 Objectives of the MTh

The objective of this thesis is to implement an isolated DC-DC converter with closed loop control scheme that complies with the specified requirements. To achieve this final objective, the following stages have to be completed:

- Clearly define the converter to build.
- Study the existing state-of-the-art solutions and carry out a critical discussion of this state of the art, to decide the best option for the project. Thoroughly examine advantages and disadvantages of each topology applied to this project. Select the topology that suits the application the most.
- Understand the principle of operation of the selected topology, perform theoretical analysis and design the converter following the theoretical design procedure.

- Carry out simulations to test the performance of the circuit, including effect of the parasitics.
- Implement the designed converter
- Test and obtain experimental validation
- Discuss the results

1.3 Methodology

To fulfill the objectives of this thesis, the following methods are used:

- The converter is defined from the requirements of the customer and industry-wide standards.
- State-of-the-art solutions from the leading industry manufacturers and scientific publications are studied and compared. Topology is selected to be suitable for the power range of 600W to 3kW.
- The selected topology is thoroughly studied and understood. Design procedure from Texas Instruments has been followed to obtain the initial design.
- Simulations are performed on PSIM, electronic circuit simulation software from Powersim. After verifying the initial design, parasitic components have been added to the simulation and design has been adjusted accordingly.
- To implement the designed converter, first components were selected. Then magnetic components were designed using Frenetic AI. Next, modular PCB was designed in Altium Designer. The modular design was chosen to make the troubleshooting stage easier.
- After the prototype PCB was printed and populated, it was tested on the stage by stage basis. E.g., first only primary side, then adding the secondary side and, lastly, adding the control circuit.

- Outcome of those tests have been studied, compared to the expected results, and discussed.

1.4 Thesis Organization

In Chapter two, converter is defined, and various topologies are analyzed. Based on the comparative analysis of the aforementioned topologies, the final converter topology is selected. Detailed resonant considerations for zero-voltage transition are discussed. Small signal analysis of selected converter is performed, and a control system is proposed.

Chapter three describes the design procedure of the selected converter power and control stages. Moreover, the validation of magnetic elements designed by Frenetic AI is performed.

In Chapter four, the design developed in Chapter three is validated through simulations, and improved where necessary.

Chapter five describes PCB layout design, selection of components, hardware implementation of magnetic components and final prototype.

Chapter six describes the experimental validation of expected results. Moreover, in this chapter, the step-by-step evolution of the converter based on the experiment results is described.

Chapter seven contains conclusions and possible future work.

Chapter 2

System definition and theoretical analysis

Given the 600W-3kW power range of the converter, and the fact that it is connected after the PFC rectifier stage, Level-1 electric vehicle charger topologies were chosen as a reference point. According to the study presented at the Energies journal [1], non-isolated DC-DC converter topologies are often used for medium and high power EV applications ($\geq 10kW$), whereas full-bridge isolated topologies are more common for applications below 10kW. Full bridge converters are the preferred option for our power range because they reduce current and voltage stresses of the semiconductor devices, relatively simple, and demonstrate higher efficiency with minimal cost impact.

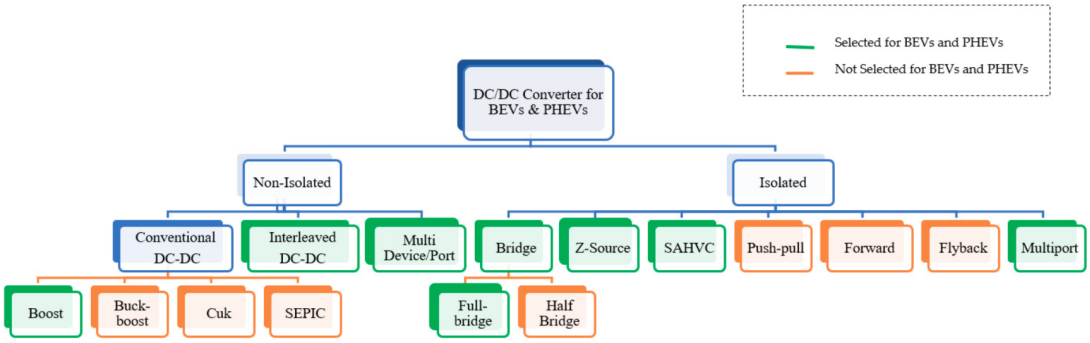

Figure 2-1: Classification of DC-DC converter topologies [1]

2.1 Comparative analysis of PSFB and FB-LLC topologies

According to Texas Instruments [3], Phase-Shifted Full Bridge (PSFB) and Full Bridge LLC (FB-LLC) are the two main topologies used for high power DC-DC conversion. These two topologies have approximately similar components count and overall excellent performance. However, they have some fundamental differences that make them suitable for different applications. In the following subsections, both of these topologies are studied, and their advantages and disadvantages discussed.

2.1.1 Full Bridge LLC resonant converter

Figure 2-2 shows Full-Bridge resonant LLC (FB-LLC) converter with a full-bridge rectifier.

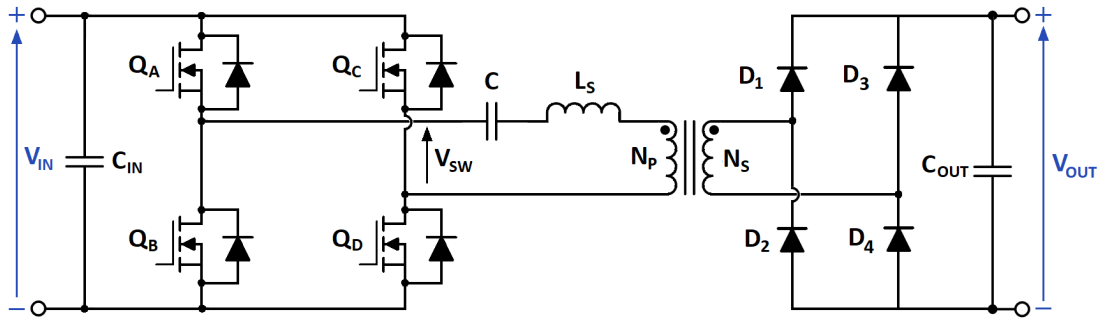

Figure 2-2: Full-bridge LLC resonant converter

Main parts of the FB-LLC converter are:

- Full bridge that consists of four semiconductor switching devices.
- Resonant tank that consists of a capacitor, series inductance and parallel inductance, that is usually the magnetizing inductance of the transformer.
- High-frequency transformer: standard or center-tap based on the rectification technique chosen.

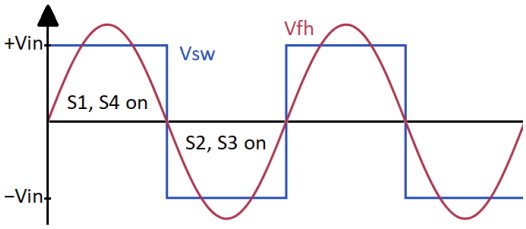

Figure 2-3: Waveforms of FB-LLC

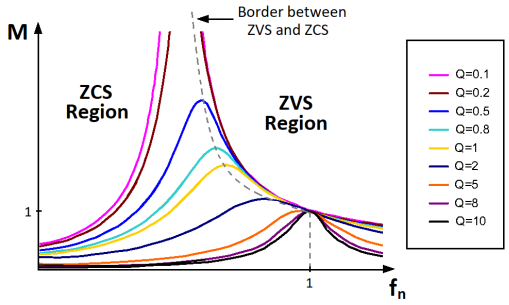

Figure 2-4: Typical gain vs. frequency plot of FB-LLC

- Full wave rectifier: full bridge rectifier or center-tap rectifier.
- Output capacitor.

Switches S1 and S4 are operated by the same control signal, while S2 and S3 are opposite to them with some dead time to allow safe transition. This switching pattern results in a square wave voltage at the output of the full bridge, which is then modeled as a sinusoidal waveform using the first harmonic approximation (Figure 2-3).

The output voltage of the Full-Bridge LLC converter is controlled by changing the switching frequency, and the gain varies with frequency as shown in Figure 2-4.

2.1.2 Phase-Shifted Full-bridge converter

Figure 2-5 shows the basic Phase-Shifted Full-Bridge Converter (PSFB). Main parts of the PSFB converter are:

- Full bridge that consists of four semiconductor switching devices. In this figure, body diode and the parasitic capacitance of each semiconductor device are shown.
- Shim inductance. In some cases, leakage inductance of the transformer can be utilized instead of a separate inductor
- High-frequency transformer: standard or center-tap based on the rectification technique chosen.

- Full wave rectifier: full bridge rectifier or center-tap rectifier.
- Output LC filter.

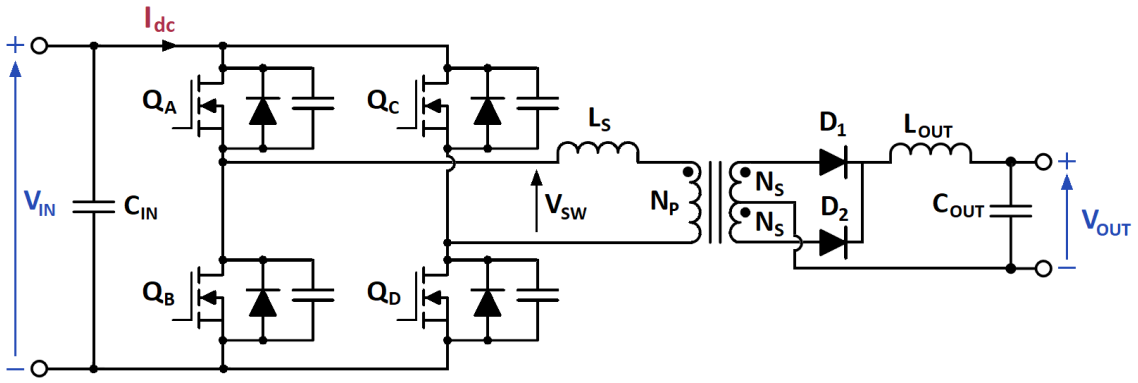

Figure 2-5: Phase-Shifted Full-bridge converter

The control of the PSFB converter is different from FB-LLC converter's. For PSFB, two sets of gate signals are used, so QA and QD are not in phase as in FB-LLC, but have a specific phase shift as shown in Figure 2-6). This phase shift is the main control parameter that changes the output voltage.

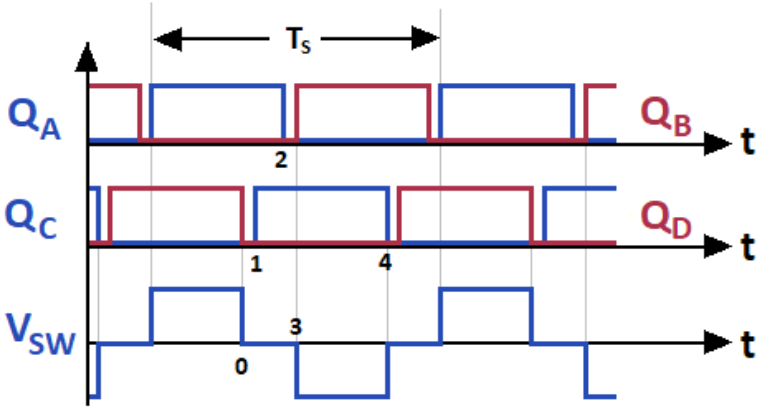

Figure 2-6: Simplified waveforms of Phase-Shifted Full-bridge converter

2.1.3 Comparison table of PSFB and FB-LLC

In the Table 2.1 summary of the comparative analysis between FB-LLC and PSFB is demonstrated.

Table 2.1: Comparison of PSFB and LLC

Aspect	**FB-LLC**	**PSFB**
Frequency	Variable, used as a control input. Therefore, synchronization, and paralleling several converters is difficult. Magnetic component design is also more complex due to the variable frequency.	Fixed, easier for synchronization. Easier to parallel several converters and share current.
Conversion ratio	Simple. Buck derived topology, output voltage can be easily derived from transformer turns ratio and the phase shift	Complex, approximate expression that is not accurate away from resonance frequency.
ZVS	Yes, but difficult at higher frequency.	Yes, ZVS is possible for all primary and even secondary side active and passive switches[5]. However, difficult at light loads, and varies for leading and lagging legs.
Light load	Uses burst mode to prevent unreasonable increase of the switching frequency.	Uses burst mode to maintain ZVS. More efficient at light load than FB-LLC
Efficiency	Good. At resonance higher than the efficiency of PSFB	Good.
Output capacitor	Large capacitor, very high ripple.	Small capacitor, low ripple.
Output filter inductor	Not used	Used, and is a considerable investment of cost, space.
Primary switches	..	RMS currents on primary switches ar higher for PSFB.
EMI	Low	Medium, EMI noise is higher compared to FB-LLC
Output voltage range	Medium	Wide range of output voltage without compromising the efficiency.
Efficiency	Good. The highest efficiency when at resonance, higher than PSFB.	Good

To conclude, Full-Bridge LLC converter topology is the best choice for the point-of-load converters, where it would operate near the resonance frequency most of the time since FB-LLC demonstrate the highest efficiency and the lowest EMI when it is at the resonance frequency. Although FB-LLC has higher efficiency and lower EMI

at the resonance point compared with the PSFB, for our application variable load performance is the most important. Therefore, PSFB topology has been selected for this power supply.

2.2 Selection of the rectifier stage topology

In this section, various options for the rectification stage are considered, advantages and disadvantages are discussed. The comparison of center-tapped and full-bridge rectifiers, and comparison of synchronous and diode rectifiers are provided in following subsections.

2.2.1 Center-tapped vs Full-bridge rectifier

Two options for the rectification stage are shown in the Figure 2-7.

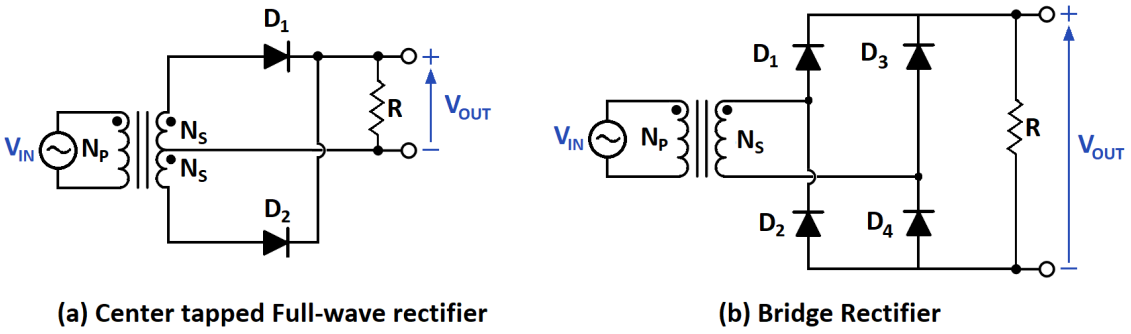

Figure 2-7: Center-tapped vs. Bridge rectifier

Both topologies shown in the Figure 2-7 are full-wave rectifiers. However, one uses center-tapped transformer and two semiconductor devices, whereas the other utilizes the standard transformer and four semiconductor devices. In the case of center-tapped rectifier, only one of the secondary windings is conducting at any given time. Therefore, the transformer size will be bigger. Moreover, the reverse voltage applied to diodes will be two times higher, compared to the bridge rectifier. Also, transformer utilization factor (TUF) is higher for the bridge rectifier case. However, the center-tapped rectifier has the advantage of using only two semiconductor devices

instead of four. Apart from cost implications, this also means that there will be a voltage drop over only one device in series with the output. Therefore it is more efficient.

2.2.2 Synchronous rectification vs. Diode bridge

Figure 2-8 demonstrates two options of center-tapped rectifier. The rectifier in Figure 2-8 (a) utilizes diodes. The diode rectifier is the most common and simple rectification technique used in medium and high power applications. The main advantages of using diode rectifier are robustness and simple implementation. However, the lower limit of voltage drop over a diode is 0.3V, and that affects the efficiency of the system.

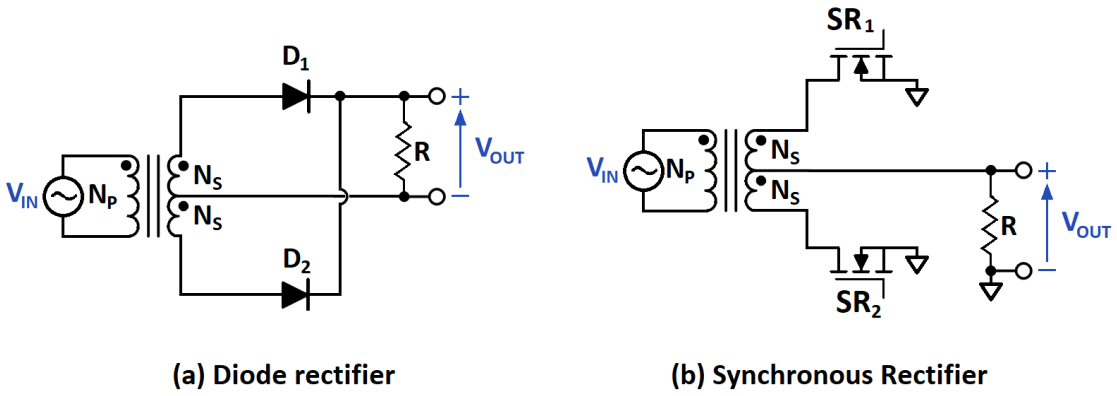

Figure 2-8: Diode rectification vs. Synchronous rectification

In synchronous rectification (Figure 2-8 (b)) MOSFETs are utilized instead of diodes. The voltage drop over MOSFETs can be decreased by lowering R_{DSon}. So for certain current levels, synchronous rectification can be more efficient. However, there is an addition of two gate drive circuits and more complex control. For this project, diode rectification is selected. However, given our modular approach, the synchronous rectification capabilities are included in the control board. The synchronous rectification can be achieved by only replacing the rectifier module.

2.3 Principle of operation of PSFB

In this section, half of the switching period will be analyzed to demonstrate and discuss the zero-voltage transition in the Phase-Shifted Full-Bridge converter as per the Application report by Texas Instruments [6]. As shown in Figure 2-6, voltage V_{SW} is divided into 4 sections in each switching period: zero volts when both upper or both lower switches are conducting, positive V_{in} when switches Q_A and Q_D are conducting, and negative V_{in} when switches Q_B and Q_C are conducting. These two intervals, when voltage is not zero, are when the power is transferred. However, since there is a deadtime between conducting periods of upper and lower switches of the same leg, there will be time (hundreds of nanoseconds) when only one switch is conducting. This short intervals of time are the key to the zero-voltage transition. Moreover, internal body diode of the FET and its parasitic output capacitance are highly instrumental in achieving ZVS. Thus, they are drawn separately in the Figures 2-9 to 2-13 and will be referred as D_A to D_D, and C_A to C_D in the description. Another thing to mention is that L_s here symbolizes lump sum of shim inductor and the leakage inductance of the transformer. The reasoning behind having a separate shim inductor or utilizing only the transformer leakage will be given in the Chapter 3. To understand the operation better, half period is divided into five intervals. Moments of time that designate the start and the end of each interval are marked in the Figure 2-6. Status of each FET and the description of the interval are given in the Table 2.2. The resulting voltage and current waveforms are given in the Figure 2-14 after the description of all stages.

Table 2.2: Time intervals of PSFB operation

Interval	Q_A	Q_B	Q_C	Q_D	*Description*
$t < t_0$	ON	OFF	OFF	ON	Initial condition
$t_0 < t < t_1$	ON	OFF	OFF	OFF	Right leg transition
$t_1 < t < t_2$	ON	OFF	ON	OFF	Clamped free-wheeling interval
$t_2 < t < t_3$	OFF	OFF	ON	OFF	Left leg transition
$t_3 < t < t_4$	OFF	ON	ON	OFF	Power transfer interval

2.3.1 Initial condition

In the Figure 2-9 below Q_A and Q_D are conducting. Thus, it is a power transfer stage. At this stage, the transformer is delivering power to the secondary side, and the diode D_1 is conducting. The description of operation starts at time t_0, when this transient finishes.

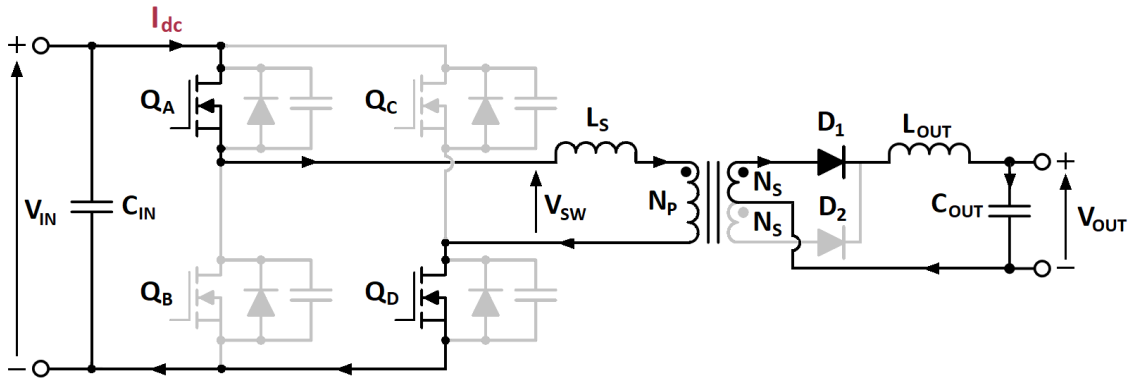

Figure 2-9: Initial condition: $t < t_0$

2.3.2 Right leg resonant transient interval

Before t_0 voltage over Q_C, and consequently C_C is equal to $+V_{in}$, and voltage over Q_D and C_D is zero. At the time t_0 the switch Q_D is turned off, that commences the right leg resonant transient interval as shown in the Figure 2-10.

When Q_D turns off, the current flowing in the primary side is kept almost constant by the shim inductor. Now, this current will have to divert, and flow using the FET's parasitic output capacitance C_D. As a result, C_D charges up to the positive input voltage value, while C_C discharges. So within this short (100-500ns) time, the resonant transition takes place. Consequently, Q_C has no drain to source voltage prior to turn on at t_1, therefore, allowing lossless zero voltage switching.

Moreover, at both t_0 and t_1 voltage at the source of Q_A is equal to the positive rail voltage, whereas the voltage at the drain of Q_D is equal to negative rail voltage at t_0 and positive rail voltage at t_1. Hence, during this transient voltage V_{SW} decreases

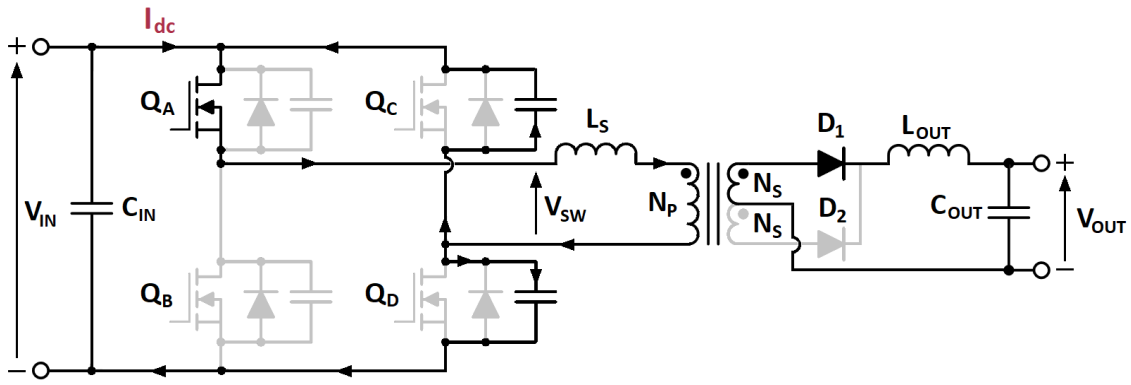

Figure 2-10: Right leg transition: $t_0 < t < t_1$

from V_{in} to zero. So at the time t_1, there is no voltage across transformer primary and secondary windings, and no power transfer.

2.3.3 Clamped freewheeling interval

After the right leg transition finishes, the voltage over Q_C is zero, and the primary current is now flowing through Q_A and D_C. At the time t_1 the FET Q_C is turned on, and the current will split between the switch Q_C and its body diode D_C. This shunts the switch impedance $R_{ds(on)}$ with the body diode, thus decreasing conduction losses. At this interval, there is no power drawn from the V_{in} source, and no power transfer. If the components were ideal, within this interval, no power would be dissipated, and the primary current would remain constant. This clamped freewheeling interval is shown in the Figure 2-11 below.

2.3.4 Left leg resonant transient interval

At the time t_2 Q_A turns off, and the current that was previously flowing through the channel of Q_A now flows through its output parasitic capacitance C_A as shown in the Figure 2-12. This current charges up the C_A, and given that the drain voltage is equal to the upper rail voltage, the voltage at the source of Q_A becomes equal to the negative rail voltage. Simultaneously, the capacitor C_B is discharged, and voltage

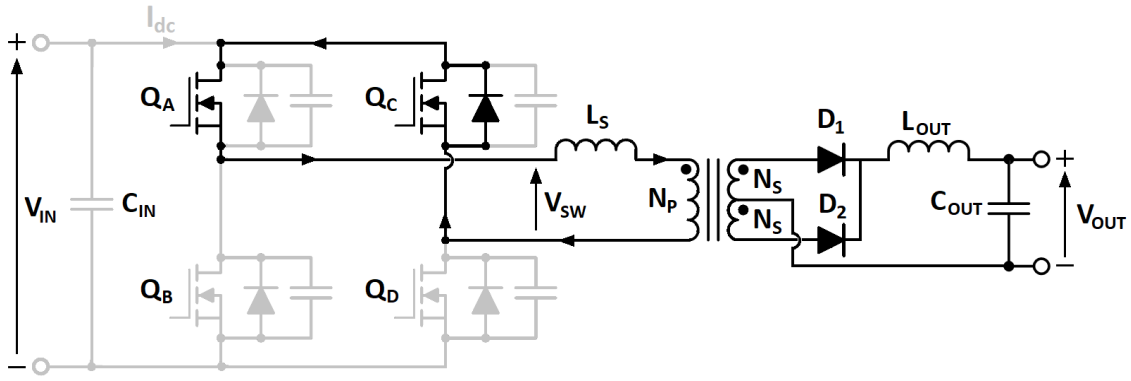

Figure 2-11: Clamped freewheeling interval: $t_1 < t < t_2$

over Q_B becomes zero, which enables zero-voltage switching for Q_B when it is turned on at the time t_2.

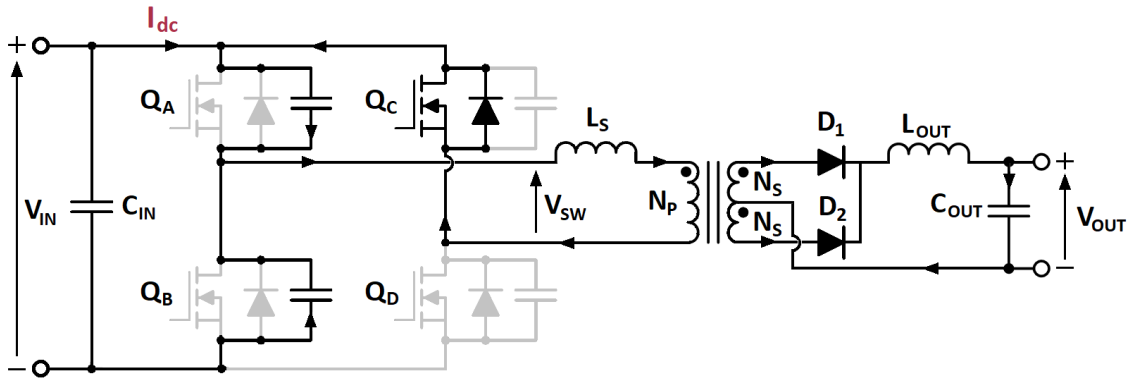

Figure 2-12: Left leg transition: $t_2 < t < t_3$

2.3.5 Power Transfer Interval

At the time t_3, when there is no voltage over Q_B, it is turned on, and that commences the power transfer interval. Two diagonal switches are conducting, and in this case, an inverted input voltage is applied over the transformer primary windings and the shim inductor (Figure 2-13). The current magnitude rises at a rate determined as a ratio of the input voltage and the series primary inductance. During this interval, the power is delivered to the load through D_2. The converter will continue to deliver

power until the switch Q_C is turned off at the time t_4. So at the time t_4, conditions are similar to those at t_0, but a different pair of diagonal switches are conducting. At that moment another right leg transient is initiated, that charges C_C and discharges C_D allowing a zero voltage turn-on of Q_D.

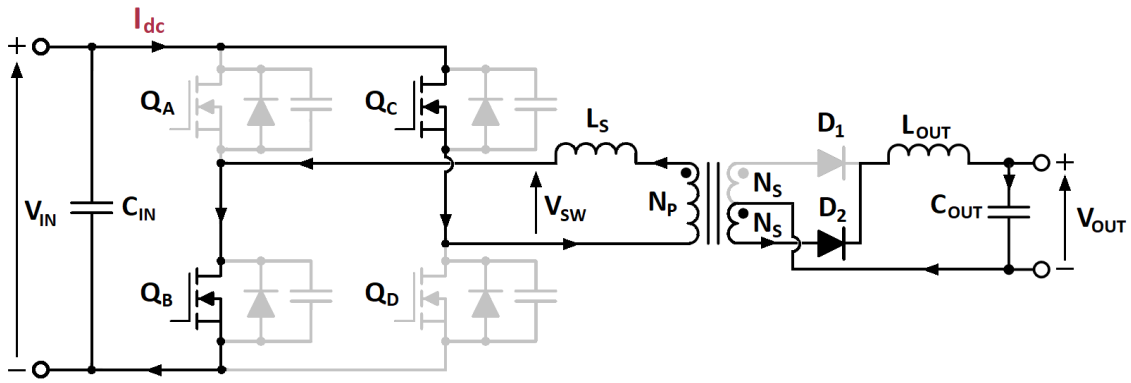

Figure 2-13: Power Transfer Interval: $t_3 < t < t_4$

Resulting voltage and current waveforms that correspond to each of the time intervals of the Table 2.2 are demonstrated in the Figure 2-14.

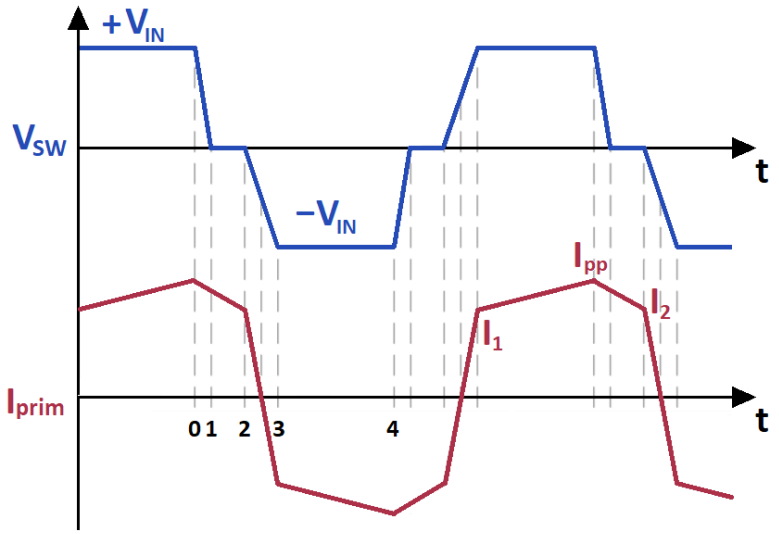

Figure 2-14: Voltage and current wavforms $t_0 < t < t_4$

It is important to note that left leg transition (turning on Q_B) will take more time than the right leg transition (turning on Q_C), because the current that is charging

and discharging the capacitors is now lower than it was during the right leg transition due to losses in the clamped free-wheeling interval. In similar way, transient for discharging Q_D takes less time than discharging Q_A. And that is visible on Figure 2-14: the voltage slope is higher after power transfer interval, and smaller after clamped free-wheeling interval.

With the switching pattern given in the Figure 2-6, Q_C and Q_D are a part of "lagging leg", and Q_A and Q_B are leading leg, because as the name implies the transients on A and B happen first (fixed), and then C and D follow (controlled). So from the transients above, it can be concluded that ZVS for lagging leg needs less time, and ZVS for leading leg needs more time [7]. This is important to remember when choosing the dead-time for ZVS.

2.4 Zero voltage transition

In this section, the conventional Zero-Voltage switching technique is discussed. However, there are studies that propose more complex systems that allow ZVS operation over a wider range of load conditions [8]. Resonant transitions that took place between $t_0 < t < t_1$ and $t_2 < t < t_3$ are key to obtaining ZVS. Essentially, ZVS was achieved by discharging and charging capacitors using the energy stored in the shim inductor within this transient time. Consequently, two main conditions must be met in order to achieve ZVS. First, the energy stored in the inductor must be enough to charge or discharge the upper and lower capacitors of the same leg. Second, this transient must be finished before the turn-on signal is given to the FET. Total equivalent capacitance during the right leg transient will be equal to

$$C_{total} = C_C + C_D + C_{tr}; \tag{2.1}$$

Where C_{tr} is the parasitic capacitance of the transformer, C_C and C_D are the average output capacitance values of the FETs Q_C and Q_D. The procedure to calculate the average value of the capacitance from the information on the FET datasheet will

be provided in the following chapter. So the total energy required for this right leg transition is

$$W_{capacitive} = \frac{1}{2} * C_{tot} * {V_{in}}^2 \tag{2.2}$$

While the energy stored in the shim inductor, including the transformer leakage inductance, is

$$W_{inductive} = \frac{1}{2} * L_s * {I_{prim}}^2 \tag{2.3}$$

So the first condition of ZVS can be summarized as

$$W_{inductive} \geq W_{capacitive} \tag{2.4}$$

Or,

$$L_s * {I_{prim}}^2 \geq (C_C + C_D + C_{tr}) * {V_{in}}^2 \tag{2.5}$$

To comply with the first requirement, the shim inductor is chosen to provide enough energy for ZVS at various load conditions. The second condition means that the delay time before turning on the FET needs to be calculated accurately to allow the full transient. One approach is to set it as

$$t_{delay} = \frac{k}{4 * f_{res}} \tag{2.6}$$

And resonant tank frequency is:

$$f_{res} = \frac{1}{2 * \pi * \sqrt{L_s * C_{tot}}} \tag{2.7}$$

The coefficient k in the equation 2.6 is 1 in [6] or increased up to 2.25 in [9] based on the empirical data. In any case, this delay time is an estimation, but in reality, the transient time will differ based on the load conditions. Therefore, there has been a number of studies that explore the option of adaptive dead time, and some control circuits have a programmable adaptive delay feature [12].

2.5 Small signal analysis of PSFB converter

Phase-Shifted Full-Bridge converter is a buck-derived topology. The output voltage is proportional to the duty cycle, which is defined by the phase shift between diagonal FETs. However, the effective duty cycle on the secondary side is actually less due to limited slope of the rising and falling primary current $\frac{V_{in}}{L_s}$. This phenomenon is called "lost duty" [13]. The Figure 2-15 demonstrates "lost duty" phenomenon via the voltage applied on the primary windings of the transformer and shim inductor V_{SW}, the voltage applied on the output filter V_{OF} and primary current I_P.

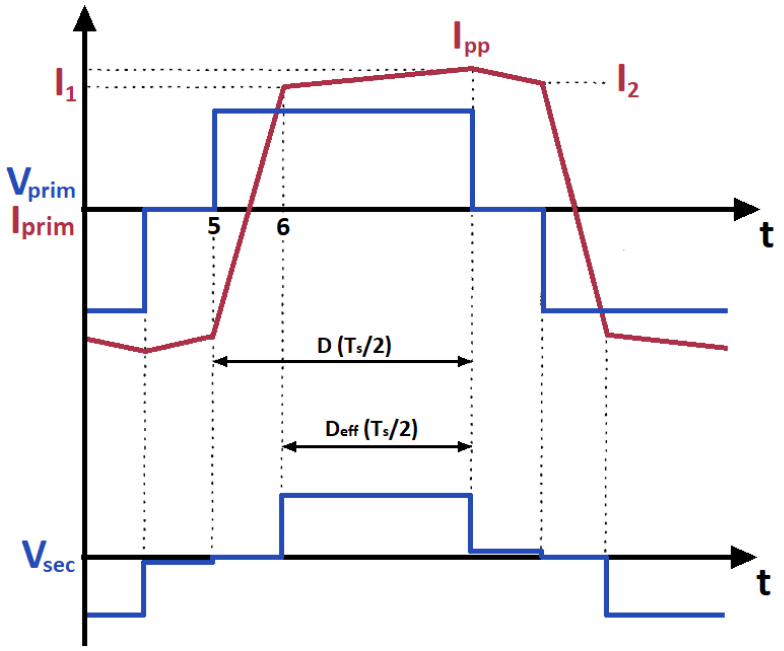

Figure 2-15: "Lost duty": Current and voltage waveforms

Since the secondary side of Phase-Shifted Full-Bridge is essentially a buck converter, the output voltage can be calculated as

$$V_o = \frac{N_s}{N_p} V_{in} D_{eff} \tag{2.8}$$

So, the effective duty cycle on the secondary side of the converter is

$$D_{eff} = D - \Delta D \tag{2.9}$$

From the slope of the rising current between t_5 and t_6 as shown in Figure 2-15:

$$\frac{\Delta I_p rim}{\Delta t} = \frac{I_1 - (-I_2)}{\Delta D * \frac{T_{sw}}{2}} = \frac{V_{in}}{L_s} \tag{2.10}$$

Which results in

$$D_{eff} = D - \Delta D = D - \frac{I_1 + I_2}{\frac{V_{in}}{L_s} * \frac{T_{sw}}{2}} \tag{2.11}$$

Where I_1 and I_2 can be defined from the slope of primary current, and substituted as in [14]

$$D_{eff} = D - \Delta D = D - \frac{N_s/N_p}{\frac{V_{in}}{L_s} * \frac{T_s w}{2}} * (2 * I_{Lo} - \frac{V_o}{L_o} * (1 - D) * \frac{T_{sw}}{2}) \tag{2.12}$$

So, from 2.12 it can be concluded that effective duty cycle D_{eff} on the secondary side of the transformer depends on the duty cycle of the primary voltage set by the control D, output filter inductor current I_{Lo}, the shim inductor value (including transformer leakage) L_s, the input voltage V_{in}, and the switching frequency f_{sw}. Therefore, the small signal transfer function of the Phase-Shifted Full-Bridge converter will depend on L_s, f_{sw}, and perturbations of the output inductor current $\hat{i}_{Lo}$, input voltage $\hat{v}_{in}$, and the duty cycle of the primary voltage $\hat{d}$. Based on that, a small-signal model of a PSFB converter has been derived in [14], and shown in Figure 2-16.

In this figure, $\hat{d}_i$ stands for the duty cycle modulation due to change in the output inductor current. According to [14] it is equal to

$$\hat{d}_i = -\frac{4 * (N_s/N_p) * L_s * f_{sw}}{V_{in}} * \hat{i}_{Lo} \tag{2.13}$$

Whereas, the duty cycle modulation due to change in the input voltage is defined as

$$\hat{d}_v = -\frac{4 * (N_s/N_p) * L_s * f_{sw} * i_{Lo}}{V_{in}^2} * \hat{v}_{in} \tag{2.14}$$

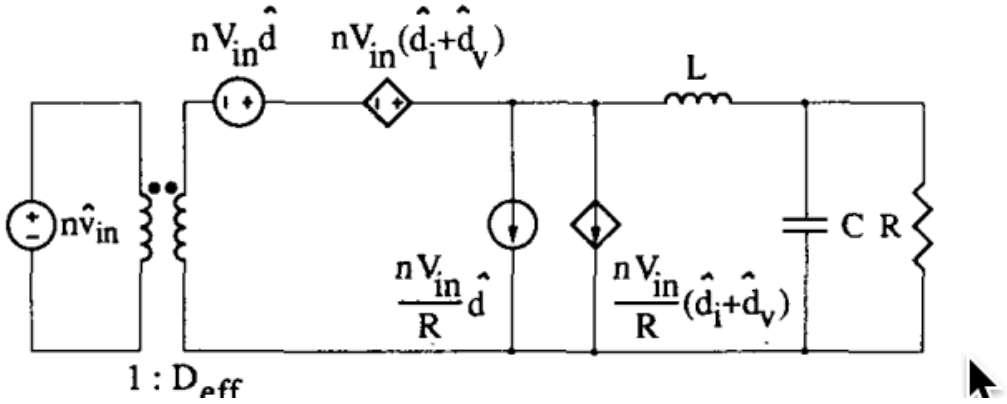

Figure 2-16: Small-signal circuit model of PSFB converter [14]

The total change of the effective duty cycle can be given by

$$\hat{d}_{eff} = \hat{d} + \hat{d}_i + \hat{d}_v \tag{2.15}$$

In Figure 2-16, the contribution of the $\hat{d}_i$ and $\hat{d}_v$ is represented by two controlled sources, and the contribution of $\hat{d}$ by two independent sources. This representation highlights that the former two originate from the converter circuit itself, and not the control circuit.

Based on the above open-loop Control-to-Output transfer function ($\hat{v}_{in} = 0$, $\hat{i}_{Lo} = 0$) is given in [14] as

$$G_{vd}(s) = \frac{\hat{v_o}}{\hat{d}} = \frac{\frac{N_s}{N_p} V_{in}}{s^2 L_o C_o + s(\frac{L_o}{R_{load}} + R_d C_o) + \frac{R_d}{R_{load}} + 1} \tag{2.16}$$

Where

$$R_d = 4(\frac{N_s}{N_p})^2 f_{sw} L_s$$

However, this model does not account for the output capacitor equivalent series resistance ESR_{Co} and losses P_{losses}. Enhanced dynamic model has been developed in [15]

$$G_{vd}(s) = \frac{\hat{v_o}}{\hat{d}} = \frac{\frac{N_s}{N_p} V_{in} R_{load}}{L_o C_o (R_{load} + ESR_{Co})} \cdot \frac{s ESR_{Co} C_o + 1}{s^2 + 2s\omega_n \xi + \omega_n^2} \tag{2.17}$$

The natural frequency ω_n is

$$\omega_n = \frac{1}{\sqrt{L_o C_o}} \sqrt{\frac{R_{load} + R_{eq} + 4(N_s/N_p)^2 f_{sw} L_s}{R_{load} + ESR_{Co}}} \tag{2.18}$$

Where R_{eq} is an equivalent resistance that represents losses

$$P_{losses} = V_{out} I_{out} \cdot \frac{1-\eta}{\eta} = R_{eq} I_{out}^2 \tag{2.19}$$

The damping ratio ξ is

$$\xi = \frac{\sqrt{\frac{L_o}{C_o}} + \sqrt{\frac{C_o}{L_o}}[(R_{load} + ESR_{Co})(R_{load} + R_{eq} + 4(N_s/N_p)^2 f_{sw} L_s) - R_{load}^2]}{2\sqrt{(R_{load} + ESR_{Co})(R_{load} + R_{eq} + 4(N_s/N_p)^2 f_{sw} L_s)}} \tag{2.20}$$

The equation 2.17 shows that control-to-output transfer function demonstrates a second order dynamic behaviour. Here gain depends on the transformer turns ratio, input voltage, load, output filter parameters and ESR of the output capacitor. G_{vd} has two poles and a zero. Zero of this system depends on the output capacitor value and its ESR. Moreover, from 2.18 and 2.20 it can be concluded that ESR of output capacitance and losses affect both natural frequency and damping of this system. Therefore, parasitics of the converter and losses cannot be ignored when modeling the system. A somewhat simplified version of this transfer function will be used in the following chapters to design the controller.

2.6 Peak current mode control

Figure 2-17 shows Phase-Shifted Full-Bridge converter with peak current mode control. The outer voltage loop compares the voltage reference with the output voltage measurement and generates an error signal. This error is then fed to a compensator, which generates peak current reference.

Current I_{dc} is measured using a current transformer, waveform is given in Figure 2-18 (top). This signal is then filtered (Figure 2-18, middle). Next, to avoid undesired

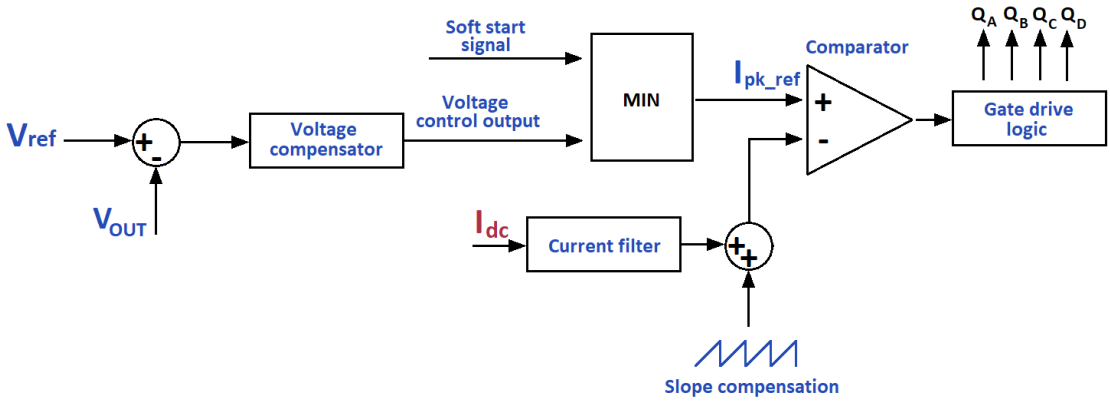

Figure 2-17: Peak current mode control - Control loops

behaviour and stability issues at duty ratio higher than 50% slope compensation is required [16]. Therefore, external ramp signal will be added to the filtered current signal as shown on the bottom graph of Figure 2-18.

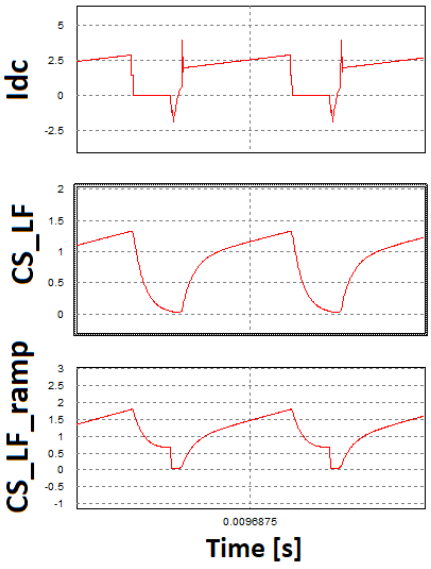

Figure 2-18: Current measurement and ramp compensation

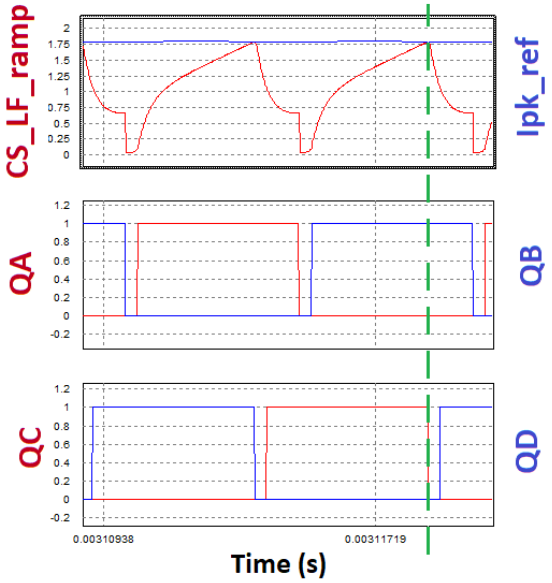

Figure 2-19: PSFB: Peak current mode control waveforms

Next, filtered current signal with slope compensation (CS_LF_ramp) is compared with the peak current reference (Ipk_ref) generated by the voltage compensator (Figure 2-19, top). The result of this comparison defines the switching logic for the FETs as in Figure 2-19. FETs Q_A and Q_B are operated at fixed 50% duty cycle (Figure

2-19, middle). When the measured current reaches the peak current reference value (green dashed line), the control system turns of the right-leg switch that was conducting (Q_C) and turns on the complementary switch (Q_B) after a sufficient deadtime. This way phase shift between right and left legs of the bridge is created.

To explain slope compensation in detail the current waveform on the switching inductor will be discussed (Figure 2-20).

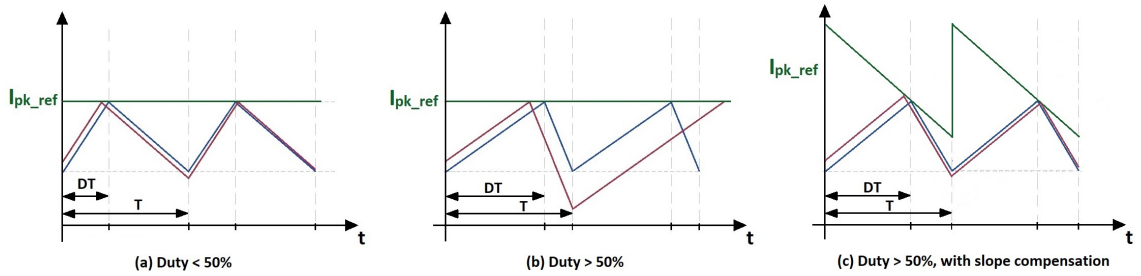

Figure 2-20: Slope compensation on switching inductor current

In Figure 2-20 (a) the duty ratio of the original waveform (in blue) is around 30%. When the positive disturbance occurs, the current limit reached earlier, which results in a small decrease of duty, and a lower level of current after period completion. On the second cycle, the current starts at a lower level, and reaches peak current reference value slightly later, resulting in longer on time, and shorter off time. At the end of the second period, the current is still higher than the original one, but for a very small amount. On the following periods, this difference diminishes making system stable again. In contrast, on the Figure 2-20 (b) the duty is around 75 %. When a similar positive disturbance is applied, instead of self-stabilizing like in the previous case, it becomes worse with every cycle. Moreover, at the end of the second cycle it did not reach peak current reference level, meaning that the switch will not turn off, and the effective switching frequency will be the half of the original. This is called "sub-harmonic oscillation", and to avoid this effect, the slope compensation is used. The behaviour of the current waveform of duty $\geq 50\%$ with slope compensation is demonstrated in the Figure 2-20 (c). This time, a ramp is added to the peak current reference value, that makes the system stabilize after positive disturbance, even with duty $\geq 50\%$. In the case of this converter, the ramp

is added to the measured signal, not the peak current reference, which essentially gives the same result. The switching inductance current waveforms are evaluated to explain the slope compensation. However, one should note that in this converter current is measured on the primary side, rather than output inductor, but the general idea of slope compensation is the same.

Another feature of the peak current mode control, present in modern control chips (for example Texas Instruments UCC28950), is a soft start. Soft start is necessary to limit transient current during the start-up procedure. It is achieved by increasing the peak reference current value gradually and at a limited rate during the start-up. The burst mode feature is present in the majority of SMPS nowadays. The main purpose of using burst mode is to increase the efficiency of the light load operation. Essentially, when the converter is at the light load and the required duty is very low, the control system just disables gate signals to the switches until the required duty reaches the certain lower threshold, after which gate signals are enabled again. This mode of operation greatly reduces the losses during light load. However, it also results in voltage fluctuations. Moreover, operating at burst mode also creates EMI issues, sometimes converter even emits audible noise.

Chapter 3

Analisys and design of the PSFB Converter

3.1 Design of the Power Stage

Main design parameters of the converter are given in Table 3.1. Design procedure, presented in [9], is followed in this section to obtain the main design parameters of the circuit.

Table 3.1: Design specifications of the power supply unit

Parameter	**Value**
Rated power	600 W
Min. input voltage	360 V
Nominal input voltage	390 V
Max. input voltage	400 V
Output voltage	300 V
Max. output voltage ripple	3 V

The switching frequency is initially set to 100kHz at the MOSFETs, which results in 200kHz ripple at the output inductor. However, this resulted in a bigger output filter inductor. Therefore, the switching frequency of 150kHz, that results in 300kHz ripple at the output inductor current has been selected. In following sections f_{sw} will stand for 300kHz.

3.1.1 Preliminary Transformer calculations

Transformer turns ratio is selected such that duty cycle is below 70% at the minimum input voltage.

$$a_t = \frac{N_p}{N_s} = \frac{(V_{INmin} - 2V_{Rdson})D_{max}}{V_o + V_d} \tag{3.1}$$

In the equation above, the V_{Rdson} is a voltage drop over the FET and considered to be 0.3V, and V_d is a voltage drop across the rectifier diode and also considered to be 0.3V. Substituting values

$$a_t = \frac{N_p}{N_s} = \frac{(360V - 2 \cdot 0.3V) \cdot 0.7}{300V + 0.3V} \approx 0.838 \tag{3.2}$$

With this turns ratio the typical duty cycle will be

$$D_{typ} = \frac{(V_o + V_d) \cdot a_t}{V_{IN} - 2V_{Rdson}} = \frac{(300V + 0.3V) \cdot 0.838}{390 - 2 \cdot 0.3V} \approx 0.65 \tag{3.3}$$

Output inductor ripple current is limited to 20% of the output current.

$$\Delta I_{Lo} = \frac{P_o \cdot 0.2}{V_o} = \frac{600W \cdot 0.2}{300} = 0.4A \tag{3.4}$$

Next, the magnetizing inductance of the transformer has to be enough to operate in current-mode control. According to [9], if L_m is too small, the magnetizing current becomes too large and will act as PWM ramp swamping out current sense signal.

$$L_m \geq \frac{V_{in} \cdot (1 - D_{typ})}{\frac{\Delta I_{Lo} \cdot 0.5}{a_t} \cdot f_{sw}} = \frac{390V \cdot (1 - 0.65)}{\frac{0.4 \cdot 0.5}{0.838} \cdot 300kHz} \approx 1.9mH \tag{3.5}$$

3.1.2 Magnetic design of the transformer

The general procedure to design magnetic components like transformers and inductors is shown in Figure 3-1. Design of magnetic elements is very complex and labour intensive exercise and it cannot be fully covered within this thesis. Thus, only the main design constraints will be discussed in this section, without detailed analysis.

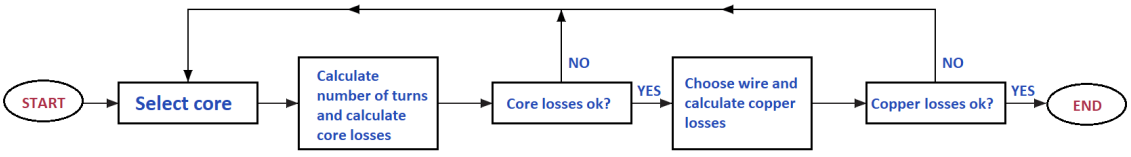

Figure 3-1: Flow chart of magnetic component design procedure

First, design criteria for the component are obtained. Based on the temperature raise limit, the maximum allowed power loss is identified. Then the core shape, size and material are selected to fulfill the requirement in 3.6 [10]

$$K_{gfe} \geq \frac{\rho \cdot \lambda_1^2 \cdot I_{tot}^2 \cdot K_{fe}^{2/\beta}}{4 \cdot K_u (P_{tot})^{((\beta+2)/\beta)}} \tag{3.6}$$

Where K_{gfe} is the core geometrical constant, β is core loss exponent, K_{fe} core loss coefficient, K_u is a winding fill factor, P_{tot} is allowed total power dissipation, ρ is the wire effective resistivity, λ_1 is applied primary volt-seconds.

Then, number of turns is chosen

$$N_p = \frac{\lambda_1}{2 \cdot \Delta B \cdot A_c} \tag{3.7}$$

Where ΔB is the peak value of the AC component of flux density, and A_c is the core cross-sectional area. The number of turns on the secondary side is obtained from the required turns ratio. Next, core losses are calculated as

$$P_{fe} = K_{fe} \cdot (\Delta B)^{\beta} \cdot A_c \cdot l_m \tag{3.8}$$

Where l_m is a magnetic path length. Generally, core losses should be limited to half of the total allowed losses. Next, wire is selected, and copper losses are calculated based on the thickness and type of the wire.

$$P_{cu} = \left(\frac{\rho \cdot \lambda_1^2 \cdot I_{tot}^2}{4 \cdot K_u}\right) \cdot \left(\frac{(MLT)}{W_A \cdot A_c^2}\right) \cdot \left(\frac{1}{\Delta B}\right)^2 \tag{3.9}$$

Where W_A is a core window area, and MLT is mean length per turn. If the copper losses comply with the requirements, then the design can be finalized.

In this project, all magnetic elements were designed using Frenetic AI. Frenetic is an artificial intelligence software, that chooses suitable core size and material, the number of windings, wire type and materials based on the estimated losses, temperature and volume constraints. Frenetic bases its decision on analytic equations, as well as on continuously learning provided by thousands of real measurements. In this subsection, Frenetic's design for the transformer will be presented and validated using loss estimation methods described in [11].

To design the transformer, the following data has been given to Frenetic:

- Primary side voltage waveform as given in Figure 2-14, with maximum value of $V_{INmax} = 400V$, duty cycle $D_{typ} = 0.65$, and the frequency of 150kHz
- Primary side current waveform as in Figure 2-14
- Target N_p/N_s ratio of 0.838
- Target magnetizing inductance L_m of 1.9mH

As a result, we have obtained a design. After optimizing the results according to the available materials, the design has been finalized as presented in Table 3.2.

Table 3.2: Design of a transformer

Parameter	**Value**
Core material	3C97
Core size	PQ32/30
Primary winding: Wire	Litz 120x0.04
Primary winding: Number of turns	20
Primary winding: Parallels	2
Secondary winding: Wire	Litz 120x0.04
Secondary winding: Number of turns	22
Secondary winding: Parallels	2

In this case, Frenetic AI has chosen it to be PQ 32/30 core made from 3C97 material of Ferroxcube [1]. The Table 3.3 contains details of the chosen core.

[1]Ferroxcube is one of the leading manufacturers of magnetic components worldwide

Table 3.3: Parameters of PQ32/30 3C97 core

	Parameter	**Value**
V_e	Effective volume	$12500mm^3$
A_c	Core cross-sectional area	$167mm^2$
W_A	Core window area	$53mm^2$
MLT	Mean length per turn	$66.7mm$
l_m	Magnetic path length	$74.7mm$
$H2$	Winding breadth	$21.3mm$

To find core losses we first need to calculate volt-seconds applied on the primary side

$$\lambda_1 = \frac{0.5 \cdot D_{typ} \cdot V_{IN}}{f_s} = \frac{0.5 \cdot 0.65 \cdot 390V}{150kHz} = 845V \cdot \mu sec \tag{3.10}$$

We can calculate maximum flux as

$$\Delta B = \frac{\lambda_1}{2 \cdot N_p \cdot A_c} = \frac{845V \cdot \mu sec}{2 \cdot 20 \cdot 167mm^2} = 126.5mT \tag{3.11}$$

The saturation flux for the 3C97 is in the range of 360mT-550mT depending on the temperature. Thus, the maximum flux of 126.5mT is within the allowed range. Based on the maximum flux and frequency, the core losses per unit of volume can be estimated as $150kW/m^3$ using the specifications of 3C97 core material provided by Ferroxcube as shown in Figure 3-2. Here the solid line shows losses at $60°C$ and dashed line at $140°C$.

Therefore, the core losses will be

$$P_{fe} = 12500mm^3 \cdot 150kW/m^3 \approx 1.9W \tag{3.12}$$

The wire chosen by the Frenetic AI is Litz 120x0.04. Litz wire is a special type of wire made of several strands (120 in this case) of smaller wires (0.04mm in diameter, 46 AWG) that reduces AC losses due to skin and proximity effect. The skin depth or penetration depth D_{pen} is defined as the distance from the conductor surface to where the current density is e times less than on the surface. It can be calculated from the frequency of AC current $f = 150kHz$, the resistivity of the material and

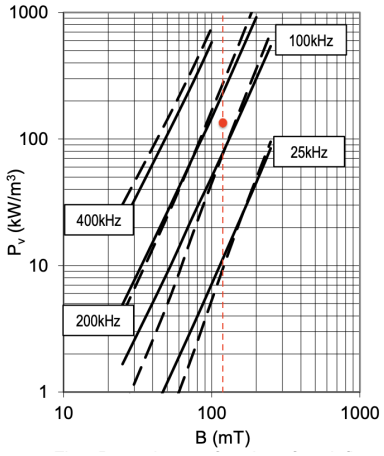

Figure 3-2: Power loss as function of peak flux density

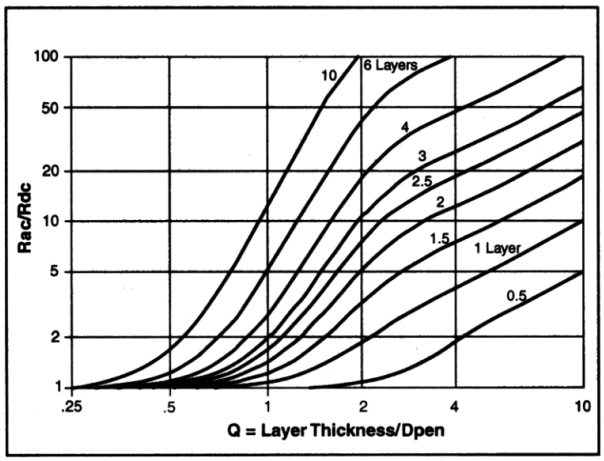

Figure 3-3: Dowell's curves for AC and DC winding losses [11]

permeability as:

$$D_{pen} = \sqrt{\frac{\rho}{\pi \mu_0 \mu_r f}} = 196 \mu m \tag{3.13}$$

A general rule of thumb is to have wire diameter less than three times the skin depth, and 46 AWG wire complies with this requirement. To estimate copper losses, the Dowell curves as shown in Figure 3-3 are used. To calculate parameter Q the winding arrangement details are required. The winding arrangement of this transformer is described in Chapter 5 (Figure 5-7). It has total of 5.5 layers, and a full layer has 24 turns. From the winding breadth given in Table 3.3, the spacing can be calculated as

$$spacing = \frac{21.3mm}{24turns} = 0.8875mm \tag{3.14}$$

The equivalent outer diameter of 120x0.04 Litz wire is approximately 0.7mm and the effective layer thickness h_{layer} is

$$h_{layer} = 0.83 \cdot dia \cdot \sqrt{\frac{dia}{spacing}} = 0.516mm \tag{3.15}$$

$$Q_{init} = \frac{h_{layer}}{D_{pen}} = 2.63 \tag{3.16}$$

However, since wire used in this case is a Litz wire with 120 strands, it can be considered as a 11x11 array of strands. Hence, the actual Q is 11 times less, around 0.24. From Figure 3-3, the R_{ac}/R_{dc} ratio at Q=0.24 for 6 layers is around 1. Next, the cross section of one AWG 46 wire is $0.0012mm^2$. The DC resistance of two parallels of 120 strands of 46AWG wire per unit of length is approximately $60m\Omega/m$. The DC resistance of each of the windings is

$$R_{DC1} = N_p \cdot MLT \cdot \frac{\Omega}{m} = 80.04m\Omega \tag{3.17}$$

$$R_{DC2} = N_s \cdot MLT \cdot \frac{\Omega}{m} = 88.044m\Omega \tag{3.18}$$

Since the DC to AC resistance ratio is 1, the above values will be used to calculate AC winding losses too. The DC and AC values of primary and secondary currents are obtained from the simulations, and equal to: $I_{DC1} = 2.245A$ (the RMS of the primary winding current), $I_{DC2} = 1.4A$ (RMS current on each of the secondary windings), $I_{AC1} = 2A$ (the RMS of first harmonic current), $I_{AC2} = 0.876A$ (the RMS of the first harmonic current for each of the secondary windings).

$$P_{cu1} = I_{DC1}^2 \cdot R_{DC1} + I_{AC1}^2 \cdot R_{AC1} = 0.723W \tag{3.19}$$

$$P_{cu2} = 2 \cdot (I_{DC2}^2 \cdot R_{DC2} + I_{AC2}^2 \cdot R_{AC2}) = 2 \cdot 0.24W = 0.48W \tag{3.20}$$

$$P_{cu} = P_{cu1} + P_{cu2} = 1.2W \tag{3.21}$$

Total losses at the transformer are approximately

$$P_{losses} = P_{cu} + P_{fe} = 3.1W \tag{3.22}$$

The field was estimated as 135mT and losses as 3W by Frenetic AI. These calculations demonstrate that the design selected by Frenetic AI is indeed valid, and

that loss and field estimations are accurate. Therefore, these calculations will not be performed for shim and output inductor.

So with this design, the transformer has been built and tested. Measured magnetizing inductance is $L_m = 2mH$, and leakage inductance $L_{lk} = 0.5\mu H$. Aspects of the hardware implementation and testing of a transformer will be discussed in the following sections. Updating the equations 3.2 and 3.3 with the actual transformer parameters

$$a_t = \frac{N_p}{N_s} = \frac{20}{22} = 0.909 \tag{3.23}$$

$$D_{typ} = \frac{(V_o + V_d) \cdot \frac{N_p}{N_s}}{V_{IN} - 2V_{Rdson}} = \frac{(300V + 0.3V) \cdot (20/22)}{390 - 2 \cdot 0.3V} \approx 0.7 \tag{3.24}$$

3.1.3 Preliminary shim inductor calculations

In order to calculate the required shim inductor value, parasitic output capacitance of the FETs must be known. For this project, IXFH20N50P3 MOSFETs were selected. The component selection is discussed in detail in the following chapters. The parasitic output capacitance $C_{OSSspec}$ is specified in the datasheet as 230pF. However, it was measured at $V_{ds} = 25V$ drain-to-source voltage. Therefore the average C_{OSSavg} needs to be calculated

$$C_{OSSavg} = C_{OSSspec} \cdot \sqrt{\frac{V_{ds}}{V_{INmax}}} = 230pF \cdot \sqrt{\frac{25V}{400V}} = 57.5pF \tag{3.25}$$

According to [9], the shim inductor value can be calculated to allow ZVS between 50% and 100% load as

$$L_s \geq (2 \cdot C_{OSSavg}) \cdot \frac{V_{INmax}^2}{\left(\frac{I_{pp}}{2} - \frac{\Delta I_{Lo}}{2 \cdot N_p/N_s}\right)^2} - L_{lk} \tag{3.26}$$

Where, I_{pp} is the peak value of the primary current that can be calculated from circuit

parameters assuming the efficiency of 90%

$$I_{pp} = \left(\frac{P_o}{V_o \cdot \eta} + \frac{\Delta I_{Lo}}{2}\right) \cdot \frac{N_s}{N_p} + \frac{V_{INmin} \cdot D_{max}}{L_m \cdot f_{sw}} \approx 3.0844A \tag{3.27}$$

Substituting values into equation 3.26

$$L_s \geq (2 \cdot 57.5pF) \cdot \frac{(400V)^2}{\left(\frac{3.08A}{2} - \frac{0.4A}{2 \cdot 20/22}\right)^2} - 0.5\mu H \approx 10\mu H \tag{3.28}$$

Even though larger $L_s + L_{lk}$ is good for the ZVS range, it decreases the effective duty ratio and creates high voltage spikes on the secondary side [18]. Therefore, ideally, we should aim for MOSFETs with lower output capacitance, that result in smaller inductance requirement for ZVS, and consequently avoid high voltage oscillations on the secondary side.

3.1.4 Magnetic design of the shim inductor

To design the shim inductor, the following data has been given to Frenetic:

- Waveform of the voltage drop over the inductor from the preliminary simulation
- Primary side current waveform as in Figure 2-14
- Target inductance L_s of $10\mu H$

As a result, we have obtained a design. After optimizing the results according to the available materials, the final design has been obtained as in Table 3.4.

Table 3.4: Design of the shim inductor

Parameter	**Value**
Core material	3C97
Core size	PQ20/16
Wire	Litz 135x0.07
Number of turns	11.5
Parallels	1
Airgap	1 mm

Implementation of the above design, the inductor of $11.3\mu H$ has been obtained. Adjusting airgap with the step of 0.5mm, it was not possible to obtain exactly $10\mu H$. Therefore, it was decided to keep it as it is, which could also be useful to balance the parasitic capacitance of the transformer which was not taken into account in calculating the total capacitance. Therefore, final $L_s = 11.3\mu H$.

3.1.5 Preliminary calculations of the output filter

Inductor L_o is designed for 20% output inductor current ripple. As in 3.4, the $\Delta I_{Lo} = 0.4A$ and the output inductor is calculated as

$$L_o = \frac{V_o \cdot (1 - D_{typ})}{\Delta I_{Lo} \cdot f_{sw}} = \frac{300V \cdot (1 - 0.7)}{0.4A \cdot 300kHz} = 750\mu H \tag{3.29}$$

Next, the output capacitor is calculated based on holdup and transient load requirements. We assume the the current step equal to 90% of the full load current, and a maximum allowed voltage transient $V_{tran} = 3V$. Maximum allowed voltage transient is selected to be 1% of the output voltage because the application of this power supply is very sensitive to voltage drops.

The full load output current is

$$I_o = \frac{P_o}{V_o} = \frac{600W}{300V} = 2A \tag{3.30}$$

Time it takes L_o to change 90% of its full load current

$$t_{hu} = \frac{L_o \cdot 0.9 \cdot I_o}{V_o} = 4.5\mu s \tag{3.31}$$

During the load transient, the more significant part of the current will go through the capacitors equivalent series resistance. Therefore, the ESR is selected for 90% of V_{tran}, while the output capacitance is selected for 10% of the transient voltage.

$$ESR_{Co} \leq \frac{V_{tran} \cdot 0.9}{I_o \cdot 0.9} = \frac{3V \cdot 0.9}{2A \cdot 0.9} = 1.5\Omega \tag{3.32}$$

$$C_o \geq \frac{t_{hu} \cdot 0.9 \cdot I_o}{V_{tran} \cdot 0.1} = \frac{4.5\mu s \cdot 0.9 \cdot 2A}{3V \cdot 0.1} = 27\mu F \tag{3.33}$$

Although the component selection will be covered in another chapter, we will need values of output capacitance and its ESR for control loop calculations. Therefore we will provide final equivalent C_o and ESR_{Co} here

$$ESR_{Co} = 321m\Omega \tag{3.34}$$

$$C_o = 495\mu F \tag{3.35}$$

3.1.6 Magnetic design of the output filter inductor

To design the output inductor, the following data has been given to Frenetic:

- Waveform of the voltage drop over the inductor from the preliminary simulation
- Output current waveform from preliminary simulation
- Target inductance L_o of $750\mu H$

As a result, we have obtained a design. After optimizing the results according to the available materials, the design has been finalized as in Table 3.5.

Table 3.5: Design of the output inductor

Parameter	**Value**
Core material	N87
Core size	E32/16/9
Wire	Litz 120x0.04
Number of turns	76
Parallels	2
Airgap	0.5 mm

Implementing above design, the inductor of $787.3\mu H$ has been obtained. Therefore, final $L_o = 787.3\mu H$.

3.2 Design of the Converter Control

The peak-current mode control described in Chapter 2 can be implemented using the analog or digital approach. For instance, the 800W and 3300W Phase-Shifted Full-Bridge converter evaluation boards from Infineon use a XMC4200 microcontroller to implement digital control of PSFB. In contrast, Texas Instruments (TI) uses their PSFB control integrated circuits (IC) with or without the integrated driver circuits. For this project, the decision has been made to make use of TI's control ICs. The solutions with integrated driver circuits were not rated for the voltage level of this converter. Moreover, it is decided to use a chip with synchronous rectification functionality to have a flexibility in the future. Therefore, TI's UCC28950 has been selected. The main functional schematic of PSFB converter utilizing UCC28950 is given in Figure 3-4.

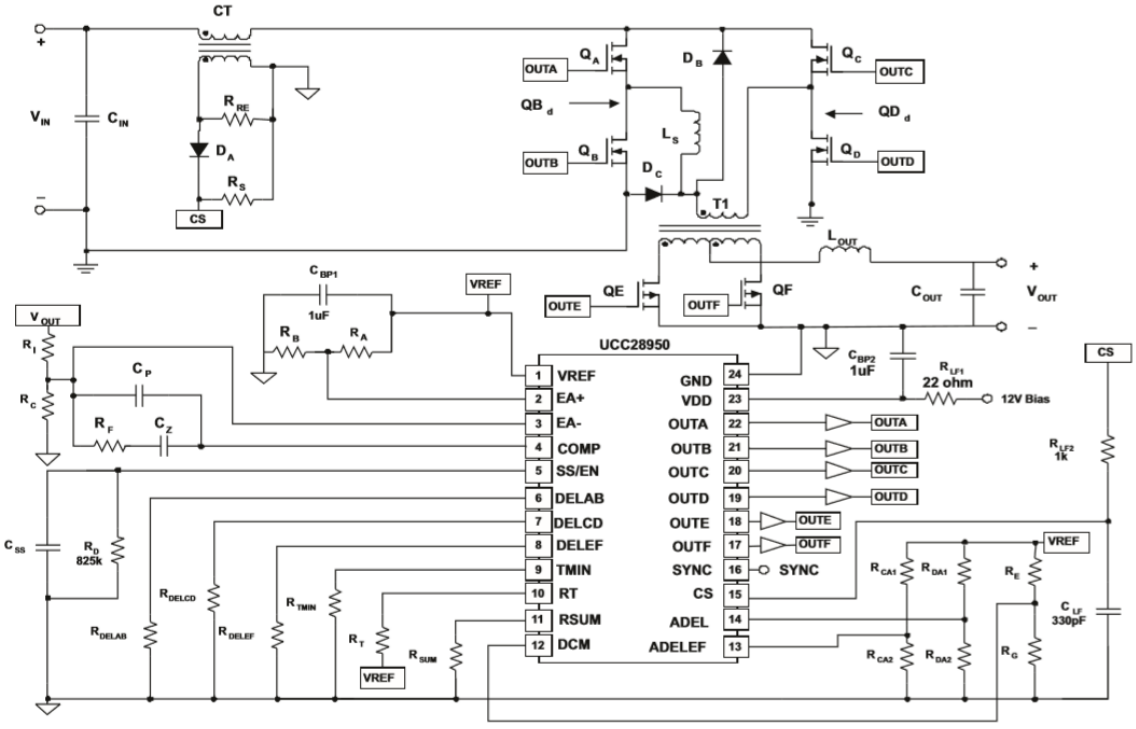

Figure 3-4: UCC28950 Phase-Shifted, Full-Bridge Functional Schematic [9]

The functional block diagram of UCC28950, shown in Figure 3-5, demonstrates the implementation of advanced control techniques discussed in Chapter 2.

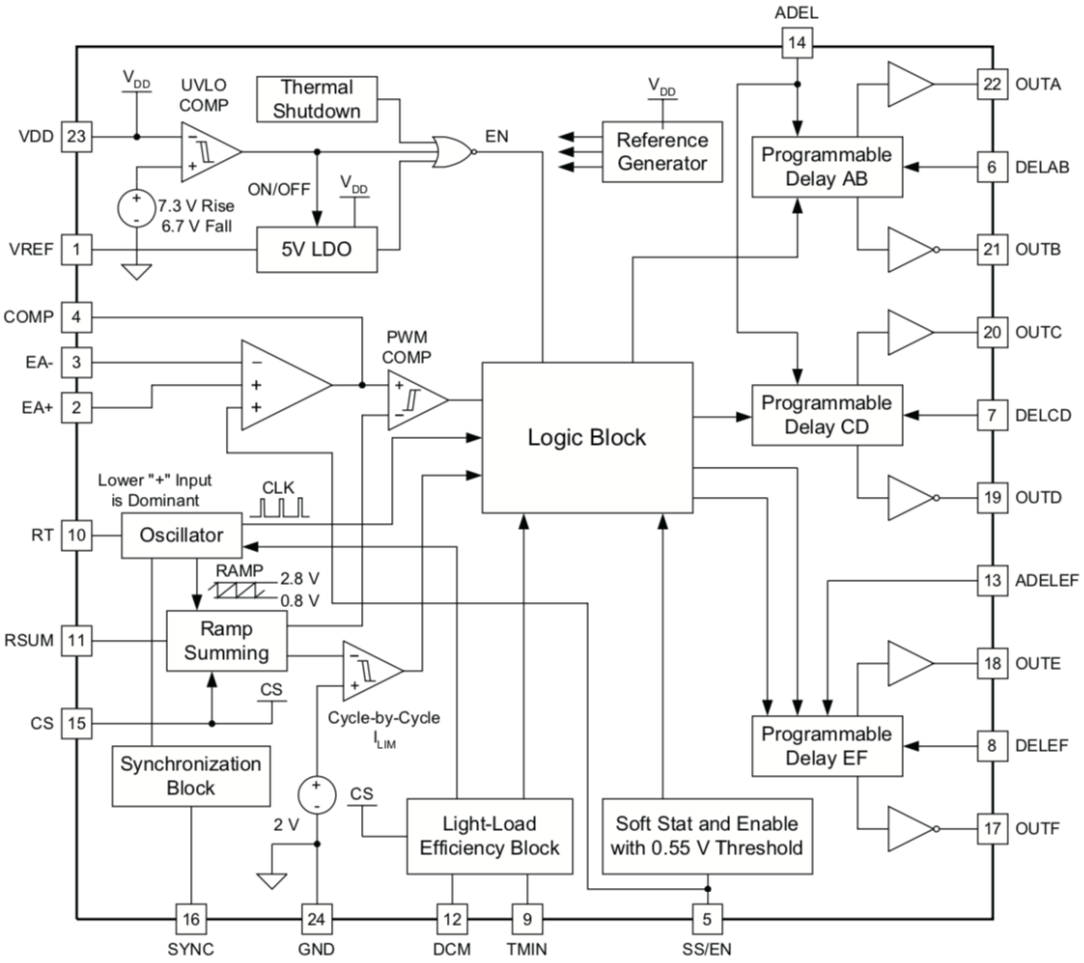

Figure 3-5: Functional Block Diagram of UCC28950 [12]

3.2.1 Current sensing network

Current in this converter is measured using a current transformer, because that allows very small losses and high bandwidth [17]. However, in our case, the measured current has an average non-zero DC value, thus, the transformer core has to be reset after each pulse. In this project reset circuit, as shown in Figure 3-4 is used. First, the current sensing transformer with $a_{CT} = N_{primCT}/N_{secCT}$ ratio equal to 100:1 is selected. Peak primary current at the minimum input voltage is calculated in equation 3.27 and equal to $I_{pp} = 3.0844A$.

In UCC28950, the voltage at which the peak current limit will trip is $V_p = 2V$. From there, the current sense resistor R_s is calculated, leaving 200mV for slope com-

pensation [9]

$$R_s = \frac{V_p - 0.2V}{\frac{I_{pp}}{a_2} \cdot 1.1} = \frac{2V - 0.2V}{\frac{3.0844A}{100} \cdot 1.1} \approx 53\Omega \tag{3.36}$$

We will choose standard resistor: $R_s = 56\Omega$ and the reset resistor R_{re} is

$$R_{re} = 100 \cdot R_s = 5.6k\Omega \tag{3.37}$$

Next, the measured current signal CS is filtered via a simple RC low-pass filter. At this stage, the filter values of $R_{lf} = 1k\Omega$ and $C_{lf} = 330pF$ have been chosen. The low frequency pole of this filter is

$$f_{lf} = \frac{1}{2\pi \cdot R_{lf} \cdot C_{lf}} \approx 482.3kHz \tag{3.38}$$

The filter can be adjusted later during the hardware implementation and testing to ensure a good balance between accuracy and bandwidth of the signal. This filtered current measurement signal is then fed to PIN15 of the UCC28950.

3.2.2 Voltage loop

For the voltage loop, the voltage measurement and voltage reference need to be provided. First, we select the voltage amplifier reference voltage at the PIN2 $EA+$ to be $V_1 = 2.5V$. This 2.5V is obtained by a voltage divider consisting of R_A and R_B connected in series and fed from PIN1 of UCC28950. This pin (VREF) is 5V, and high frequency bypass capacitor $C_{BP1} = 1\mu F$ is connected in parallel with it to filter out high frequency noise. R_A and R_B are set to $2.2k\Omega$. Another voltage divider R_C and R_I is used to scale 300V output of the converter into a 2.5V signal. To do that, R_C is set to $2.2k\Omega$, and R_I is calculated from that

$$R_I = \frac{R_C \cdot (V_o - V_1)}{V1} = \frac{2.2k\Omega \cdot (300V - 2.5V)}{2.5V} = 261.8k\Omega \tag{3.39}$$

A resistor $R_I = 261k\Omega$ is selected. The voltage compensating loop is designed based on a simplified version of equation 2.17 for control-to-output transfer function pro-

vided in [9]

$$G_{vd}(s) = \frac{\Delta V_o}{\Delta V_c} = a_t \cdot a_{CT} \cdot \frac{R_{load}}{R_s} \cdot \left(\frac{1 + s \cdot ESR_{Co} \cdot C_o}{1 + s \cdot R_{load} \cdot C_o} \right) \cdot \frac{1}{1 + \frac{s}{2\pi \cdot f_{pp}} + \left(\frac{s}{2\pi \cdot f_{pp}} \right)^2} \quad (3.40)$$

Where f_{pp} is a double pole frequency of $G_{vd}(f)$

$$f_{pp} = \frac{f_{sw}}{4} = \frac{300kHz}{4} = 75kHz \quad (3.41)$$

The load impedance R_{load} is calculated for 10% load conditions

$$R_{load} = \frac{V_o^2}{P_o \cdot 0.1} = \frac{(300V)^2}{600W \cdot 0.1} = 1.5k\Omega \quad (3.42)$$

Voltage loop is compensated with Type-2 feedback network that consists of capacitors C_P, C_Z and a resistor R_F as shown in Figure 3-4. Compensation gain is calculated as

$$G_c(s) = \frac{\Delta V_c}{\Delta V_o} = \frac{s \cdot R_F \cdot C_Z + 1}{s \cdot (C_Z + C_P) \cdot R_I \left(\frac{s \cdot C_Z \cdot C_P \cdot R_F}{C_Z + C_P} + 1 \right)} \quad (3.43)$$

The voltage loop feedback resistor R_F is calculated based on the cross-over frequency of the voltage loop. For now, croos-over frequency is chosen to be a tenth of the double pole frequency

$$f_c = \frac{f_{pp}}{10} = \frac{75kHz}{10} = 7.5kHz \quad (3.44)$$

$$R_F = \frac{R_I}{G_{vd}(f_c)} \quad (3.45)$$

To find $G_{vd}(f_c)$ for the equation above, we substitute s by $2\pi f_c$ in 3.40

$$G_{vd}(f_c) = a_t \cdot a_{CT} \cdot \frac{R_{load}}{R_s} \cdot \left(\frac{1 + 2\pi f_c \cdot ESR_{Co} \cdot C_o}{1 + 2\pi f_c \cdot R_{load} \cdot C_o} \right) \cdot \frac{1}{1 + \frac{f_c}{f_{pp}} + \left(\frac{f_c}{f_{pp}} \right)^2} \approx 0.532 \quad (3.46)$$

So, the calculated value of R_F is

$$R_F = \frac{R_I}{G_{vd}(f_c)} = \frac{261k\Omega}{0.532} = 490.5k\Omega \quad (3.47)$$

Standard resistor value of $R_F = 560k\Omega$ is chosen. Next, the feedback capacitor C_Z is calculated to increase phase margin:

$$C_Z = \frac{1}{2\pi R_F \cdot \frac{f_c}{5}} \approx 190pF \tag{3.48}$$

Capacitor of slightly higher standard value 220pF is chosen. Then, we put a pole at twice crossover frequency

$$C_P = \frac{1}{2\pi R_F \cdot f_c \cdot 2} \approx 19pF \tag{3.49}$$

A standard capacitor of $C_Z = 22pF$ is selected. The loop gain as a function of frequency is calculated as

$$T_V dB(f) = 20log(|G_C(f) \cdot G_{vd}(f)|) \tag{3.50}$$

The theoretical frequency response plot obtained from a Texas Instrument design tool for UCC28950 is shown in Figure 3-6. Please note, that the phase margin in this

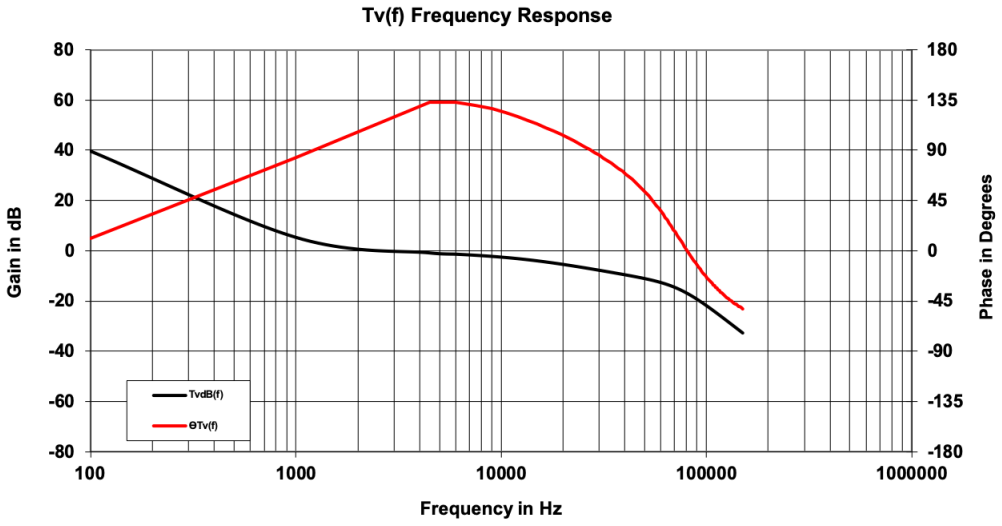

Figure 3-6: The theoretical frequency response of the converter

plot, unlike the standard Bode plots, is calculated as a distance to zero degrees at the crossover frequency. From the plot it is seen that the theoretical crossover frequency

of the voltage loop is around 2.8kHz, and the phase margin at that point is around 125° at 10% load and rated input and output voltages.

3.2.3 Soft start

The next step in designing the control system for Phase Shifted Full Bridge converter, is to set up the soft start. The soft start time is set by connecting a capacitor to PIN5 of UCC28950 as shown on 3-4. For this project, initial soft start time is set as 15ms, and the soft start capacitor is calculated as

$$C_{ss} = \frac{t_{ss} \cdot 25\mu A}{V_1 + 0.55} \approx 123nF \tag{3.51}$$

The standard capacitor of 120nF is selected.

3.2.4 Deadtime considerations for zero-voltage switching

Based on the values of average output capacitance of selected MOSFETs and the sum of shim inductance and transformer leakage inductance, the resonant tank frequency can be calculated as

$$f_R = \frac{1}{2\pi\sqrt{(L_s + L_{lk}) \cdot (2 \cdot C_{OSSavg})}} \approx 4.32MHz \tag{3.52}$$

The deadtime between complementary FETs of the same leg, when both of them are turned off, is calculated based on the empirical data as

$$t_{ABSET} = \frac{2.25}{4 \cdot f_R} \approx 130ns \tag{3.53}$$

In UCC28950 if the required deadtime is less than 155ns, then voltage V_{ADEL} at PIN14 must be 1.8V. As demonstrated in Figure 3-4 voltage at PIN14 is set via a voltage divider that is connected to $V_{REF} = 5V$. Therefore, we choose $R_{DA1} = 8.25k\Omega$, and calculate

$$R_{DA2} = \frac{R_{DA1} \cdot V_{ADEL}}{5V - V_{ADEL}} = 4.64k\Omega \tag{3.54}$$

Next, resistor R_{DELAB} is calculated

$$R_{DELAB} = \frac{t_{ABSET} - 5ns}{ns} \cdot \frac{(0.15V + V_{ADEL} \cdot 1.46) \cdot 10^3}{5} \cdot \frac{1}{1A} = 69.45k\Omega \quad (3.55)$$

We selected $68k\Omega$ standard resistor for both R_{DELAB} and R_{DELCD}.

3.2.5 Burst mode

During the light load operation, the control system might require very small duty ratio, which results in lower efficiencies during the light load operation. Therefore, the minimum duty ratio on time $t_{min} = 100ns$ is defined, and if the requested on time (power transfer interval time) is smaller than t_{min}, the FETs do not turn on. This mode of operation is called Burst mode and is set up by a resistor R_tmin connected to PIN9 of the UCC28950

$$R_{tmin} = \frac{(t_{min} - 15ns) \cdot 10^3}{6.6ns} = 12.9k\Omega \quad (3.56)$$

A standard $12k\Omega$ resistor is selected. Next, the operating frequency of the converter has to be specified via R_T resistor. For 300kHz at the output inductor current (150kHz switching for the MOSFETs), the R_T is chosen to be $38.3k\Omega$.

3.2.6 Slope compensation

The advantages of slope compensation has been discussed in Chapter 2. In UCC28950, the slope compensation is set up via resistor R_{sum} connected to PIN11.

$$R_{sum} = \frac{2.5V \cdot 10^3\Omega}{V_{slope} \cdot 0.5\mu s} \quad (3.57)$$

Where V_{slope} is a required slope compensation measured in volts per second. When setting up the current sensing network, 200mV [2] was left for the slope compensation.

[2] 10% of the maximum current sense signal $V_p = 2V$

So the minimum slope compensation is 200mV per one inductor switching period

$$V_{slope_{min}} = 200mV \cdot f_{sw} = \frac{60mV}{\mu s} \tag{3.58}$$

Next, the slope compensation is calculated based on the change in the output inductor's current and magnetizing current

$$V_{slope_{calc}} = \frac{\left(\frac{\Delta I_{Lo}}{2a_t} - \Delta I_{Lm}\right) \cdot R_s \cdot f_{sw}}{a_{CT} \cdot (1 - D_{typ})} \tag{3.59}$$

Where $\Delta I_{Lo} = 0.4A$ as calculated previously, and

$$\Delta I_{Lm} = \frac{V_{IN} \cdot (1 - D_{typ})}{L_m \cdot f_{sw}} = 195mA \tag{3.60}$$

So, substituting into 3.59

$$V_{slope_{calc}} = \frac{\left(\frac{0.4A}{2 \cdot 0.909} - 0.195A\right) \cdot 56\Omega \cdot 300kHz}{100 \cdot (1 - 0.7)} = \frac{14mV}{\mu s} \tag{3.61}$$

Since calculated slope is less than the minimum, we use the minimum slope value to calculate R_{sum}

$$R_{sum} = \frac{2.5V \cdot 10^3\Omega}{\frac{60mV}{\mu s} \cdot 0.5\mu s} \approx 83.3k\Omega \tag{3.62}$$

A resistor of $82.5k\Omega$ is selected.

Chapter 4

Validation through simulations

PSIM circuit simulation software package by Powersim is used to simulate the power converter operation. The Phase-Shifted Full-Bridge converter example is available at the PSIM libraries. Using this simulation and adapting it to the converter designed in this project, the converter operation has been simulated. Moreover, PSIM proved to be very accurate in simulating the effect of parasitic components and highly useful in identifying potential problems of the design as demonstrated in this section.

4.1 Open Loop operation

4.1.1 Original circuit

Figure 4-1 shows the original design using the parameters calculated in Chapter 3. We will denominate this simulation as "Simulation-1". To control this circuit, four gate signals are generated with a deadtime of 130ns as calculated in Chapter 3, and a phase shift that corresponds to the duty ratio of 0.85. Although the typical duty ratio is 0.7, it had to be readjusted to 0.85 to accommodate for "duty loss" phenomenon as discussed in Chapter 2. The primary side voltage and current waveforms are presented in the Figure 4-2 (a). Their shape is as expected from the design stage. And Figure 4-2 (b) demonstrates the ZVS. As we can see, the QD turns on, when its drain-to-source voltage is zero. However, in this simulation the parasitic capacitance of the secondary

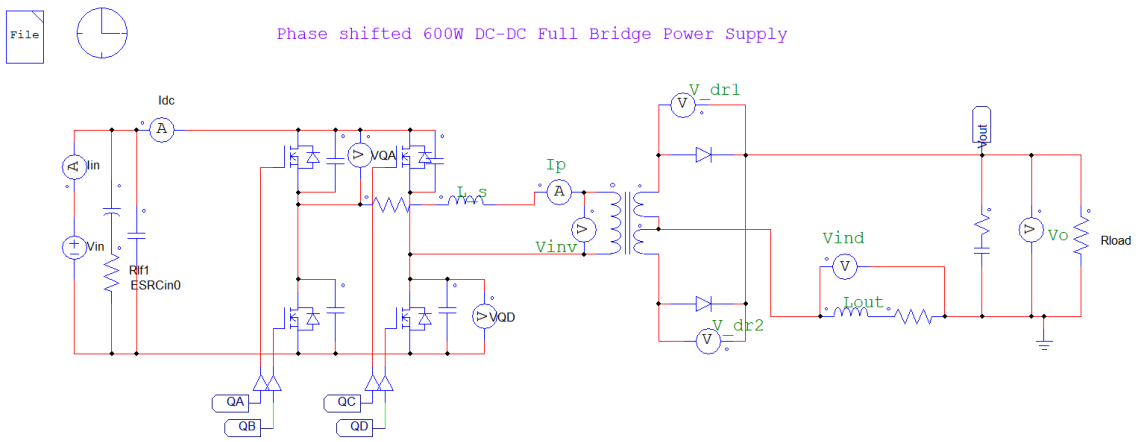

Figure 4-1: Simulation-1: Power stage

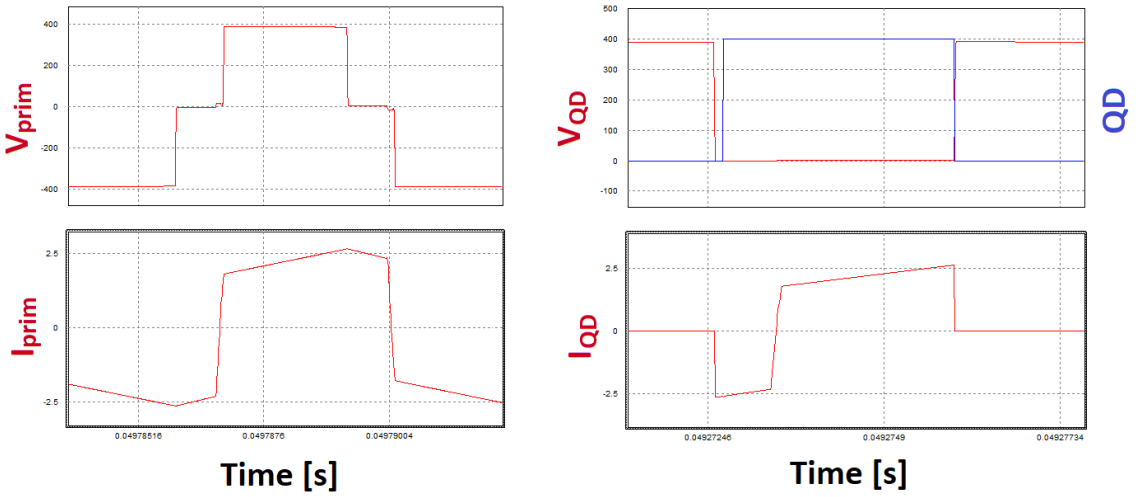

Figure 4-2: Simulation-1: Primary current and voltage, and switching of QD

side diode is not taken into account. When it is added into the circuit, the waveforms change and become as in Figure 4-3. This happens because of the resonance between the lump sum inductance $L_s + L_{lk}$ and the parasitic capacitance of the secondary side diodes. These oscillations increase the rating of rectifier diodes, cause output voltage noise and electromagnetic interference problems [19]. In this case, the maximum value of the voltage on the primary side is around 750V, and the voltage over the rectifier diode is $2 \cdot (N_s/N_p) \cdot V_{Pmax} = 1650V$, whereas the original design must have been around 880V, almost twice less. The solution to this problem is presented in [20] and Texas Instruments UCC27714EVM-511 600W Phase-Shifted Full-Bridge Converter

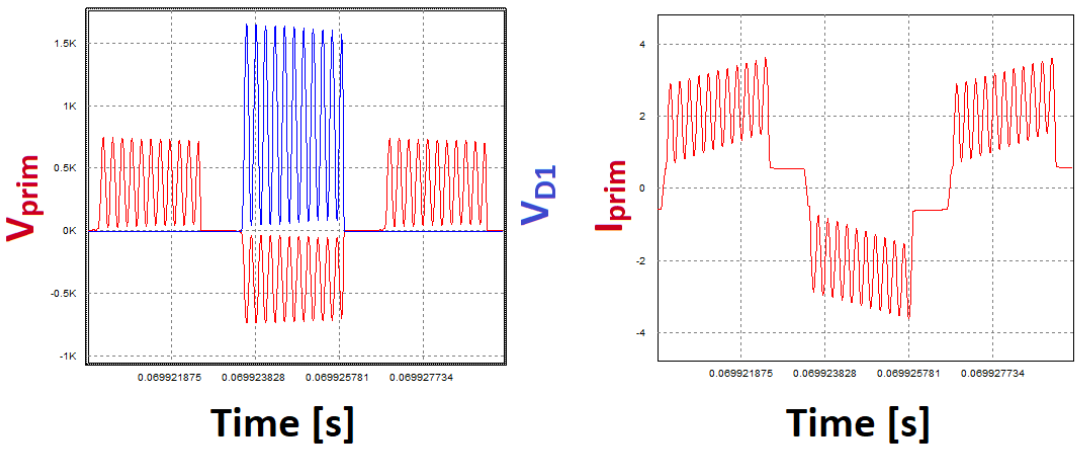

Figure 4-3: Current and voltage waveforms with diode parasitic capacitance

evaluation board [21]. An implementation of this snubber circuit is explained in the next subsection.

4.1.2 Re-designed circuit

To decrease the oscillations that appear from the resonance between $L_s + L_{lk}$ and rectifier diode parasitic capacitance, two diodes are added to the circuit: one from the negative rail to the connection point between shim inductor and transformer, and another from the connection point to the positive rail as shown in Figure 4-4. No changes have been made to the control circuit.

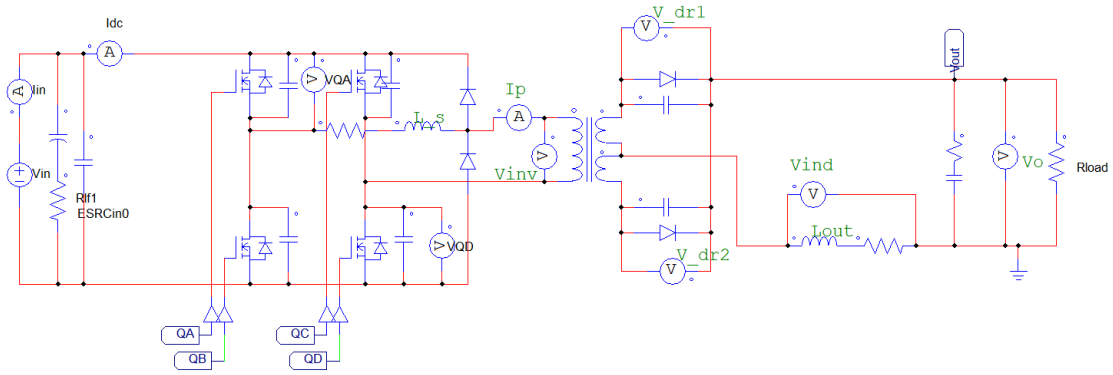

Figure 4-4: Simulation-2: Power circuit with added snubber diodes

As shown in Figure 4-5, the oscillations on the primary voltage are practically

non-existent, with small oscillation on the primary current. Moreover, the maximum voltage applied to the rectifier diodes is below 1000V. With this, we can continue to the closed loop operation simulations.

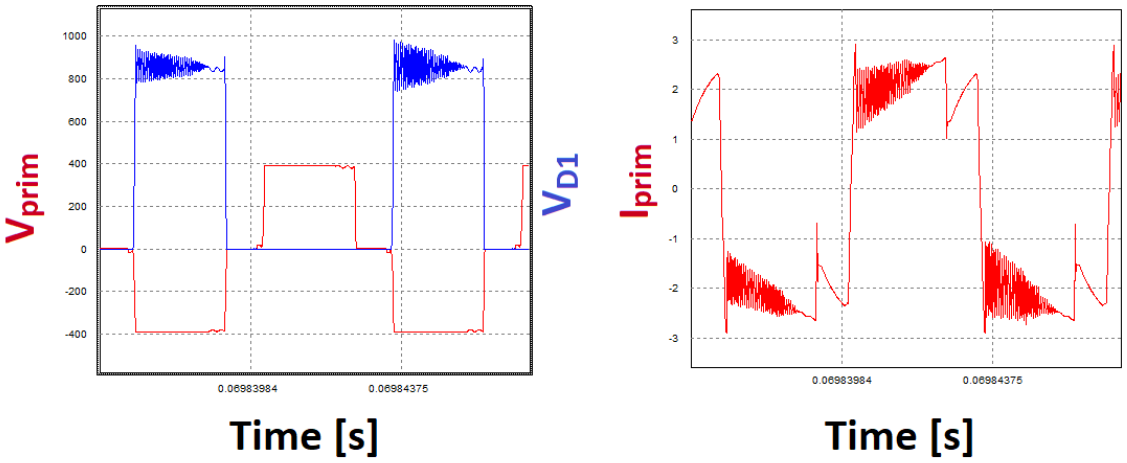

Figure 4-5: Current and voltage waveforms with added snubber

4.2 Closed Loop operation

The closed loop simulation is built based on the example provided by Powersim, using the parameters calculated in Chapter 3. In the power stage presented in Figure 4-6, the current sensing network has been added.

On the control circuit presented in Figure 4-7, we can identify the components for voltage measurement such as voltage set-point reference, voltage loop compensation, soft start, current filter, slope compensation, current loop comparator, and gate signal generation.

Figure 4-8 demonstrates how primary side current and voltage change within 50ms time frame after starting. In open loop operation, the voltage reaches setpoint within 20ms, but the peak primary current goes up to almost 40A. With the closed loop operation, the setpoint is reached at around 50ms, with the maximum transient current below 7A.

The Figure 4-9 shows soft start. The soft start logic in UCC28950 is implemented

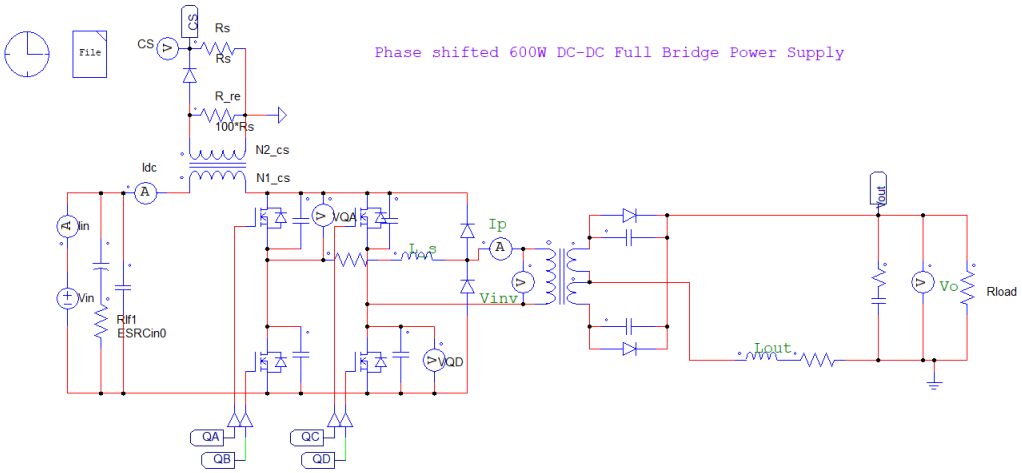

Figure 4-6: Simulation-3: Power stage

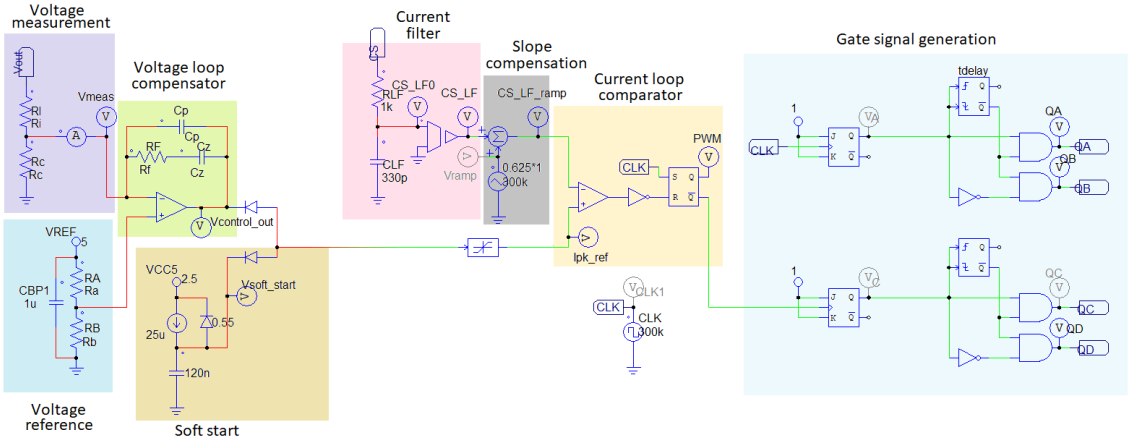

Figure 4-7: Simulation-3: Closed loop control circuit

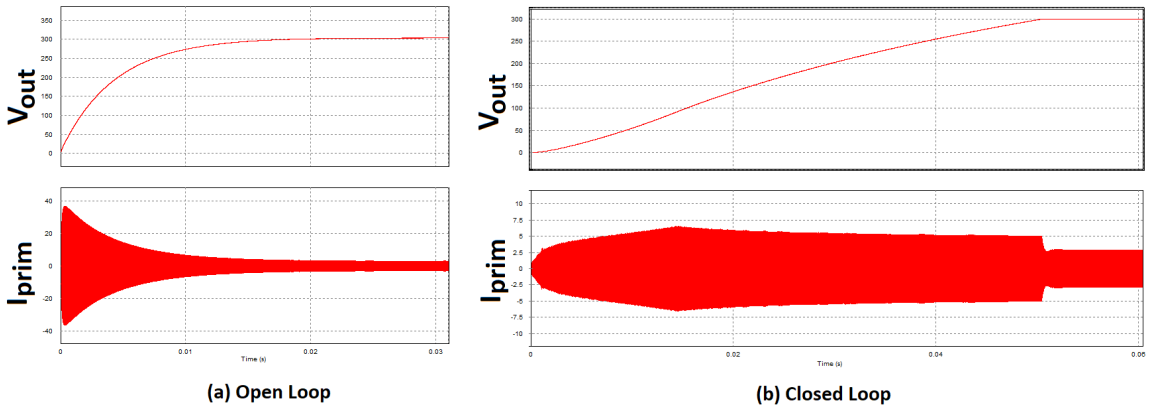

Figure 4-8: Comparison of primary current and voltage transients

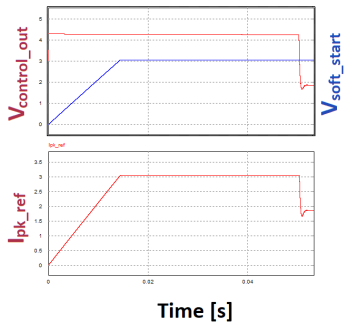

Figure 4-9: Soft starting waveforms

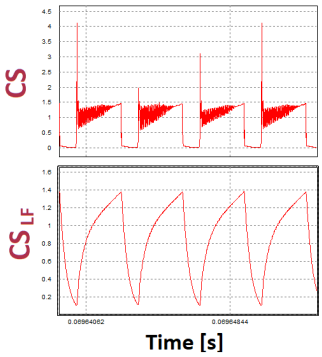

Figure 4-10: Current measurement filtering

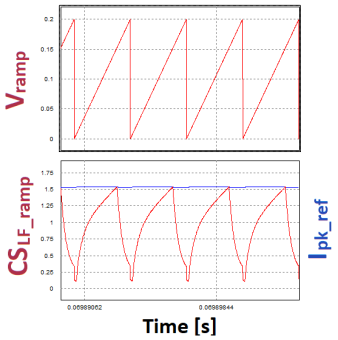

Figure 4-11: Slope compensation

in a way, that the comparator in Figure 3-5 uses the smaller out of two signals of PIN2 (represented by $V_{control\_out}$ in Figure 4-9) and PIN5 (represented by V_{soft_start} in Figure 4-9). Therefore, a peak current reference signal I_{pk_ref} is then compared with the measured current signal. Also, with 120nF capacitor, the soft start interval is around 15ms as designed.

In Figure 4-10, the measured current signal oscillates due to the resonance between rectifier diode capacitance and the inductance on the primary. After filtering and adding the ramp (Figure 4-11 top) the final waveform (Figure 4-11 bottom) is compared to the peak current reference signal.

4.2.1 Disturbance rejection

This converter will be operating at the fixed output voltage reference. Therefore, the reference tracking is not its main feature. Disturbance rejection is more important for this power supply, especially when the output load is varying. In order to examine how the system responds to the changes in load, the simulation is started with 600Ω load, which is equivalent to 25% power, 150W. Then after the system reaches steady state, load step from 25% to 100% is applied.

The resulting voltage and current transients are presented in Figure 4-12. At the moment when the load step is applied, the output voltage drops to 299.4V but quickly recovers within 2ms.

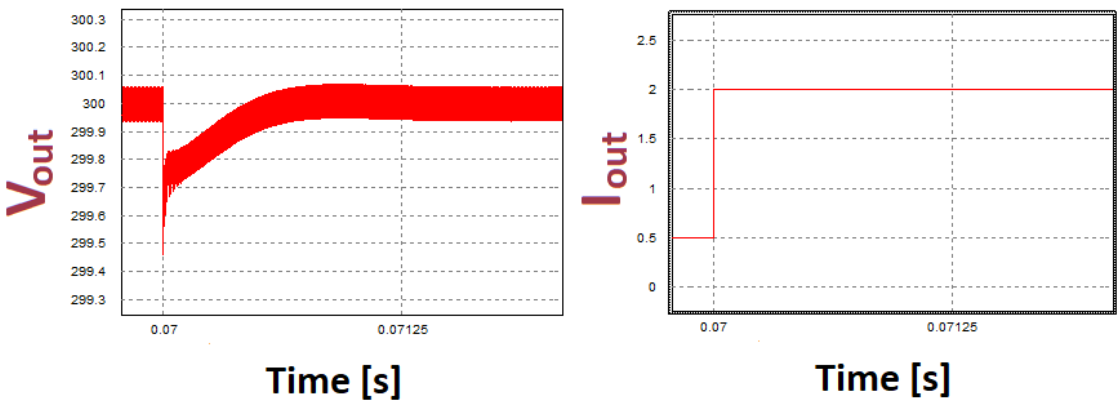

Figure 4-12: 25% to 100% load step response

4.2.2 Leading-leg vs. Lagging-leg transients

As discusses in Chapter 2, the transients of the leading leg and lagging leg MOSFETs differ. The discharging of parasitic capacitors of the leading leg MOSFETs (QA,QB) takes more time because the current over the shim inductor is lower and less energy is available to obtain ZVS.

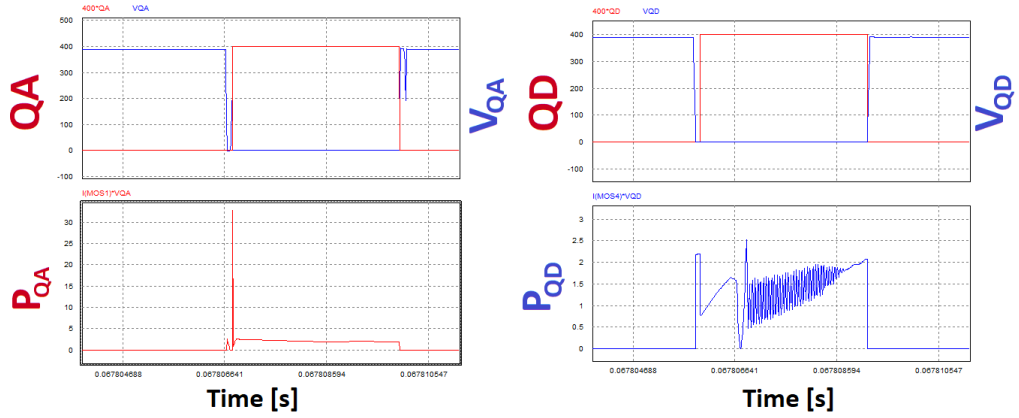

Figure 4-13: Switching transients and instantaneous power losses of leading and lagging leg MOSFETs

Plots on the right show switching of the QD (lagging leg MOSFET) along with instantaneous losses on the QD at the rated conditions with dead-time of 130ns for both legs. The ZVS is achieved, and average power loss over QD is equal to 0.7W. Plots on the left show the equivalent waveforms for QA (Leading leg MOSFET). Both turn-on and turn-off of QA are associated with voltage spikes and dips, and average

power loss over QA is equal to 1.05W. To solve the problem of different dead-time requirements of the leading and lagging legs to achieve ZVS, UCC28950 allows to specify differing dead-times for each leg. Moreover, UCC28950 has a capability to adapt the dead-time for QC and QD.

Chapter 5

PCB Implementation and built prototype

5.1 PCB general design procedure

The PCB for this converter was developed in several stages using Altium Designer software. First, the modular approach was used, which means we had four separate PCBs. One for the primary side that contained: input connection terminals, input capacitance, full bridge and snubber diodes. Second PCB for housing magnetic components: shim inductor and the transformer. Third PCB for the rectifier diodes, output inductor and capacitor, output connection terminals. And the final fourth PCB for the control chip UCC28950, and all of its related circuitry. This method of building the converter has proven to be highly effective for prototyping, because each part of the circuit can be tested independently from each other, and replaced if necessary, which made testing and troubleshooting much easier. However, due to limited space, in this section, we will discuss only the last version of the PCB, which is presented in the Figure 5-1. In this implementation, there are two PCBs: power stage and control stage. Please note that control card and the fans are not installed in this picture.

Even though it has been considered as 390V to 300V converter throughout this thesis, the actual output of the power supply is $\pm 150V$. Therefore access to the

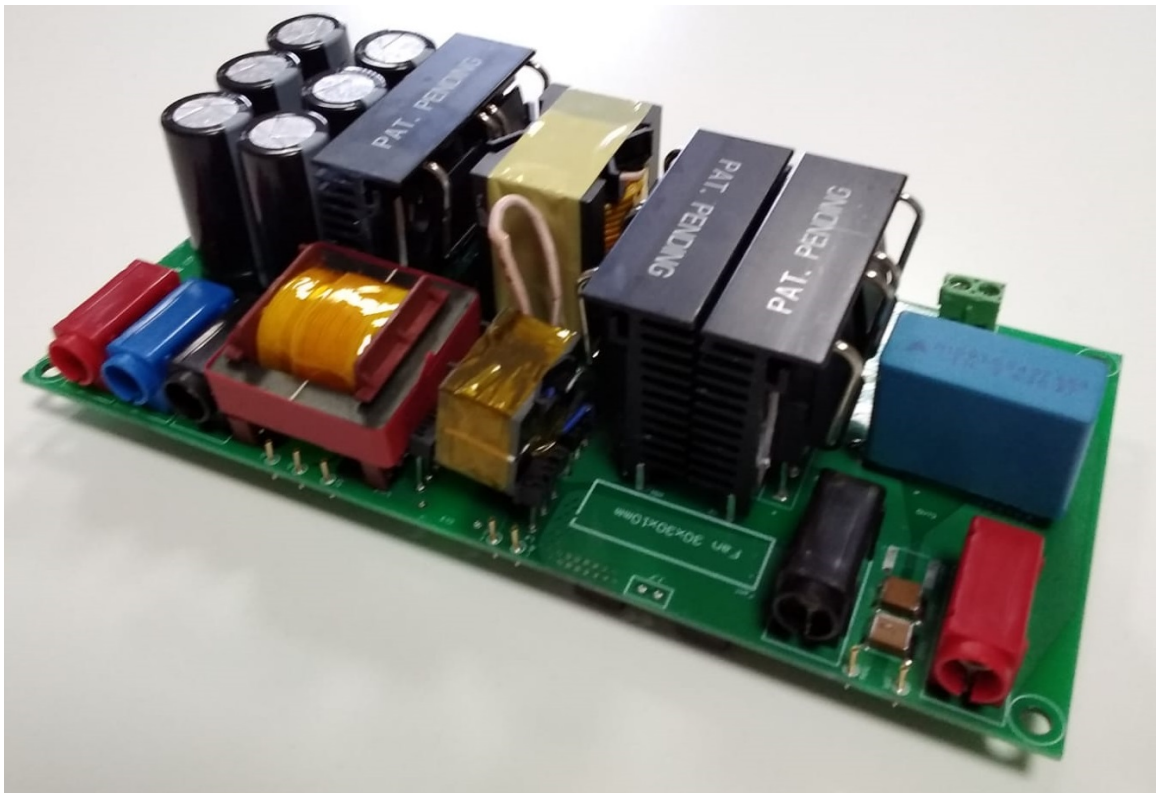

Figure 5-1: Assembled 600W power supply PCB

midpoint output voltage is added (blue connector). Moreover, the required output capacitance has been created via 6 electrolytic and 6 MLCC capacitances connected in series and parallel, as shown in Figure 5-2. Several test-points were added to the circuit, to make troubleshooting and testing easier.

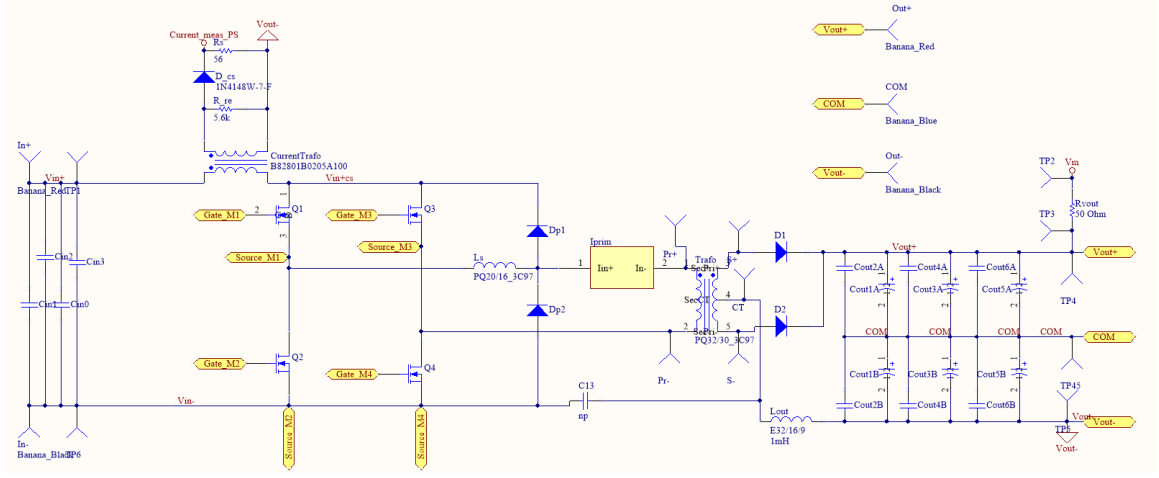

Figure 5-2: Schematic of the Power stage in Altium Designer

The driver circuit for the full bridge has been one of the most challenging parts of the design. There have been several iterations and failed attempts in implementing the driver circuit. The final driver circuit design (PCB3) that proved to be robust enough is shown in the Figure 5-3.

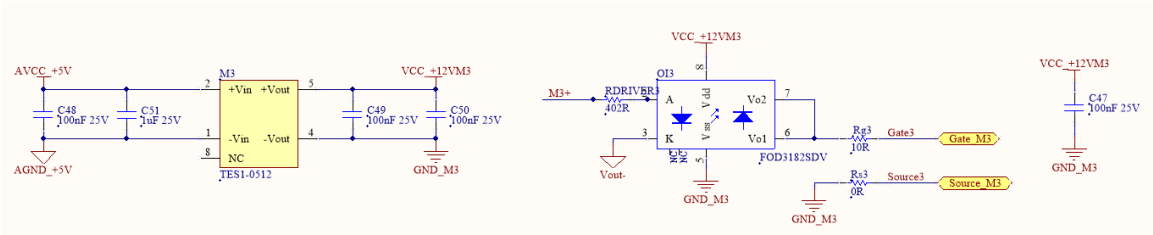

Figure 5-3: Schematic of the driver circuit in Altium Designer

Each of the four driver circuits uses an optocoupler with individual isolated 12V power supply, and several capacitors to filter out the noise. Gate resistor values have been selected according to guidelines from the MOSFET datasheet. The value of resistor R_{DRIVER} is selected such that current is enough to drive the optocoupler when connected to the control IC or the open loop signal generator.

The control PCB has been designed following TI's application note guidelines strictly. Therefore its layout repeats the design shown in [21], with the only difference being a resistor to connect the Bode 100 vector network analyzer to check loop stability. Setup and results of this stability check are discussed in detail in Section 6.2.3.

5.2 Component selection

Components for this converter were selected based on several criteria:

- Voltage and current ratings obtained from PSIM simulations. As a rule of thumb, voltage and current ratings were selected to have at least 25% extra.
- Availability on the market. The preference was given for new, but well-established components, that have been present on the market for a while and that will most likely continue to be manufactured.

- Easily replaceable. So that even if that component is not available anymore, there would be more items from different manufacturers with similar footprint and characteristics.

- Easily scalable, so that the PCB could have been used for higher power rated converter, by just choosing higher rated components of the same footprint.

For the reasons described above, and taking into account component availability at the Frenetic laboratory, footprints for components were finalized as:

- TO-247-3 for MOSFETs

- TO-247-2 for rectifier diodes

- 1206 for all SMD resistors used in the control PCB

- 0805 for all SMD capacitors used in the control PCB

In the Table 5.1 main components and their parameters are given. For confidentiality reasons, the entire bill of materials (BOM) cannot be attached to this document. Moreover, all the magnetic components are custom made, thus, they will be covered in a different section.

Table 5.1: Main components for the 600W PSFB converter

N	**Component**	**Description**
1	Full bridge MOSFETs	MOSFET N-Ch. 500V 20A TO-247
2	Rectifier diodes	SiC diode 1700V 5A TO-247-2
3	Snubber diodes	Schottky diode 600V 5A Ultrafast SMC
4	Main input capacitor	Film capacitor 10.0uF 10%
5	Output capacitor electrolytic	Capacitor alum. 330uF 20% 200V
6	Output capacitor MLCC	MLCC, 0.22uF, 200V, 1206
7	Optocoupler	3A Optocoupler 5kV 1-Ch. 8-SMD
8	12V isolated source	Isolated DC-DC 5V to 12V
9	Control IC	UCC28950

5.3 PCB layout

Switching power supplies are one of the major sources of EMI due to fast-changing voltages and currents [22]. Even though soft switching is able to reduce those emissions, there is still EMI noise that appears due to parasitic components of the converter. According to [23] there are the number of parasitic components that appear in the circuit:

- Equivalent series resistance (ESR), inductance (ESL) of the capacitors
- Capacitance between windings of the inductors and transformers
- Leakage inductance of the transformer
- Parasitic capacitance of MOSFETs and diodes
- Parasitic inductance and capacitance of the resistor
- Resistance, inductance and capacitance of the PCB tracks

The parasitic components of MOSFETs, diodes and capacitors that affect the dynamic performance of the power supply have been taken into account in the design stage of this converter. However, the last item on the list above depends largely on the PCB layout. To minimize the effect of these parasitics on the converter performance, several rules have to be followed.

- Minimize inductance of tracks that belong to loops with high current change rate, because inductance at high di/dt tends to cause voltage spikes. In phase-shifted full-bridge MOSFET and diode currents have high di/dt rate and those loops are shown in blue in Figure 5-4. There is no straightforward way to estimate the stray inductance, however, the general rule is to keep track length as short as possible.
- Minimize capacitance of switched nodes because currents proportional to the stray capacitance flow between the switched node and other circuit nodes. The switched nodes of PSFB are shown as red dots on Figure 5-4. To minimize their

capacitance, total conductor area at this node should be small, which means short and narrow tracks.

- High frequency signal tracks should be as short as possible.

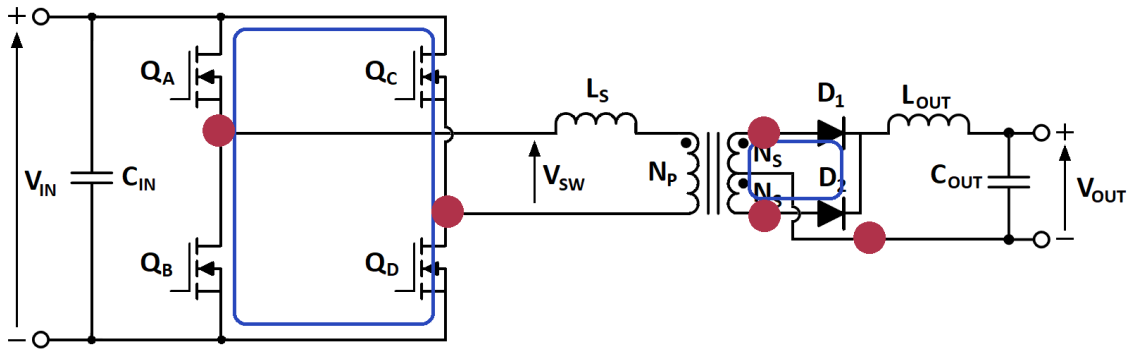

Figure 5-4: High di/dt loops and high dv/dt node

Following rules described above, two-layer printed circuit board has been designed for the power stage (Figure 5-5). Apart from minimizing the loops and nodes, extra care was taken to make sure to have good airflow for heatsinks, to have MLCC output filter capacitors right under the electrolytic ones, add stand-offs, keep signals as far away from power tracks as possible. Also, the loops in the gate driver circuit have been taken into account.

In designing the layout of the control card, guidelines given in UCC28950 application note have been followed [9]. Main points in creating the layout of the control PCB were:

- C_Z and C_P as close to PIN4 "COMP"as possible
- C_lf as close to PIN15 "CS" as possible
- High frequency switching signals away from sensitive analog signals
- Very good grounding
- C_{bp} as close to PIN1 "VREF" and PIN24 "GND" as possible

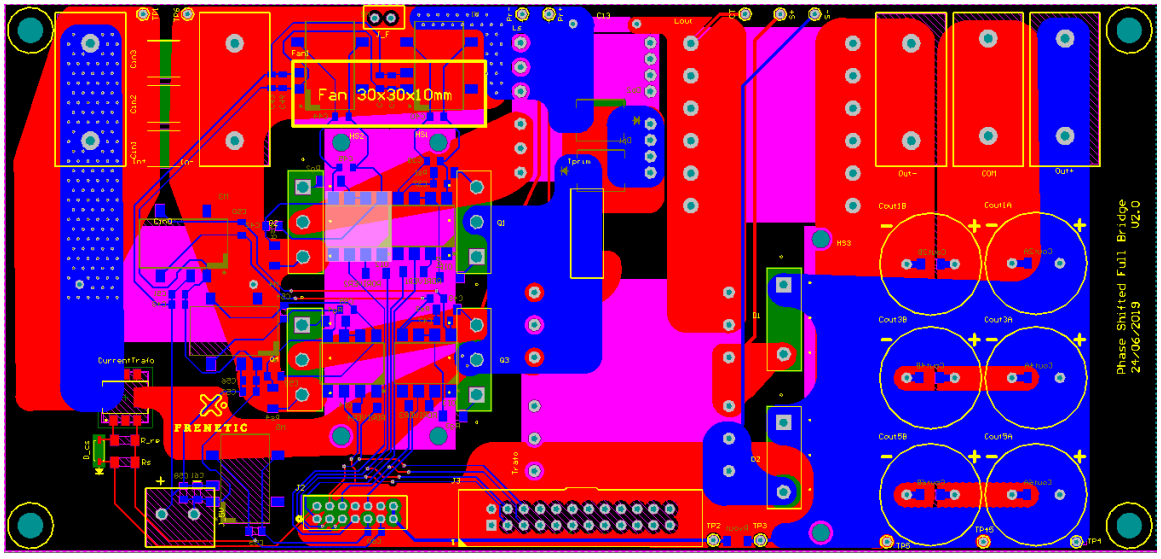

Figure 5-5: Power stage PCB layout on Altium Designer

- High frequency signal tracks as short as possible

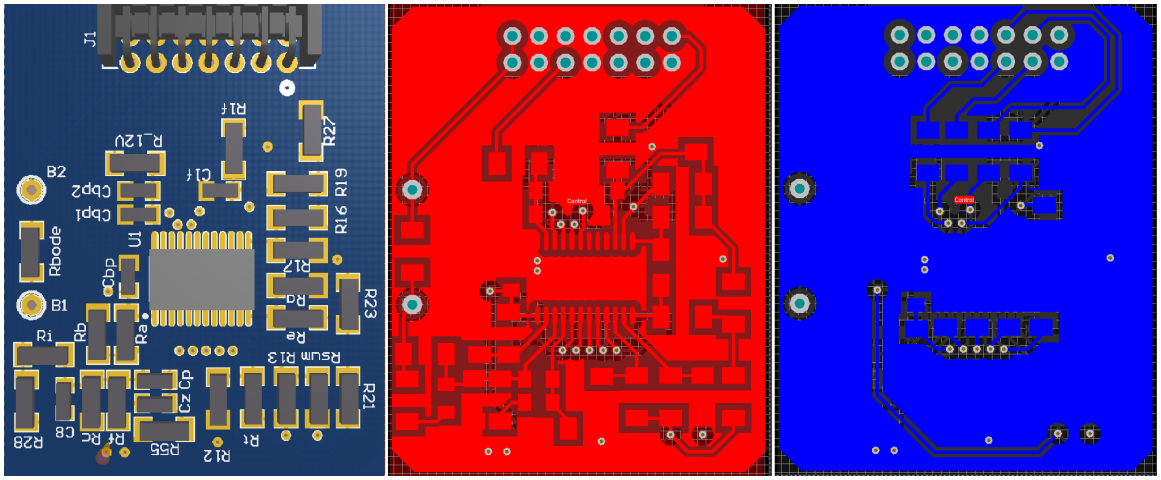

Figure 5-6: Control PCB layout on Altium Designer (3D, top, bottom)

5.4 Hardware implementation of magnetic components

The design of magnetic elements was obtained from Frenetic AI. However, it had to be readjusted according to material availability. Moreover, after the first test,

the winding temperature was increasing too fast. Therefore, a slightly bigger cross section wire has been selected, and verified via Frenetic AI. The final selected and implemented design is given in Table 3.2. The interleaved winding technique was used to minimize the leakage inductance of the transformer: 6 wires (2 parallels of primary, secondary1 and secondary2) were held together and wound on the coil former as shown in Figure 5-7.

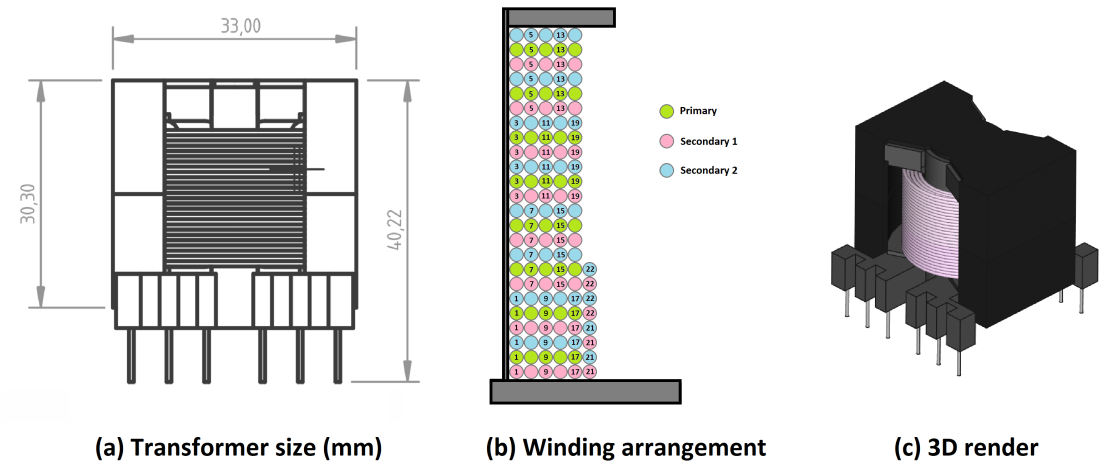

Figure 5-7: Transformer: (a) Coil Former (b) Winding arrangement (c) 3D render

Although the interleaving technique allows minimizing the leakage, it also creates isolation issues. There is a minimum required degree of isolation between transformer primary and secondary sides to comply with safety standards. When the primary and secondary windings are on separate layers of the transformer, additional isolation layer, like Kapton® polyimide films, can be added between them. When interleaving is used, it is not possible to use the aforementioned films. Therefore, higher isolation grade wires have to be selected.

After building this transformer, the next important step is to characterize it. To measure the DC resistance of the windings, a constant current is applied to the winding, and the voltage drop is measured using a very accurate sensor. To measure the magnetizing and leakage inductance, a slightly more complex measurement procedure using Bode 100 was followed, as shown in Figure 5-8. First, six different measurements were taken as per Table 5.2.

Figure 5-8: Measuring impedance using Bode 100

Table 5.2: Measurement conditions for transformer L_m and L_{lk}

N	Measured at	Condition	Impedance	Equivalent
1	Pri+ to Pri-	Secondary side open circuit	2.029mH	$L_m + L_{lk}$
1	Sec+ to CT	Primary side open circuit	2.402mH	$(L_{lk} + L_m)/a_t^2$
1	CT to Sec-	Primary side open circuit	2.399mH	$(L_{lk} + L_m)/a_t^2$
1	Pri+ to Pri-	Secondary side short circuit	510nH	L_{lk}
1	Sec+ to CT	Primary side short circuit	657nH	L_{lk}/a_t^2
1	CT to Sec-	Primary side short circuit	663nH	L_{lk}/a_t^2

Then, from this, the magnetizing and leakage inductances have been calculated. The final values were as given in the Table 5.3. The measured DC resistances are very close to the ones calculated in Chapter 3: $R_{DC1} = 80.04m\Omega$ and $R_{DC2} = 88.044m\Omega$ as per Equations 3.17 and 3.18.

Table 5.3: Measurement results for transformer

Parameter	Value
Magnetizing inductance at the primary side	$\approx 2mH$
Leakage inductance at the primary side	$\approx 0.5\mu H$
DC resistance of primary winding	$\approx 79m\Omega$
DC resistance of Sec+ to CT winding	$\approx 87m\Omega$
DC resistance of CT to Sec- winding	$\approx 87m\Omega$

The shim inductor was implemented according to Table 3.4. The size, winding arrangement, and 3D rendering of the final products is given in the Figure 5-9. The 11.5 windings of the inductor are spread over layers as 6 and 5.5 turns.

The output inductor was implemented according to Table and 3.5. The size, winding arrangement and 3D rendering of the final products is given in the Figure 5-10. The 76 turns (two parallels each) of the output inductor have been distributed

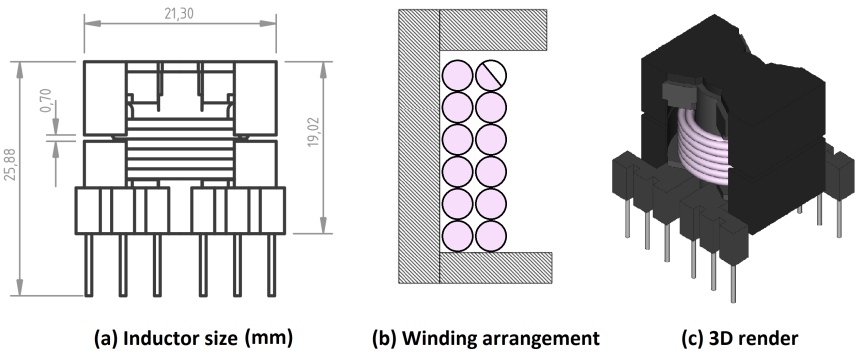

Figure 5-9: Shim inductor implementation

on 6 layers as 13 (x2) on the first five layers, and 11 (x2) on the sixth layer.

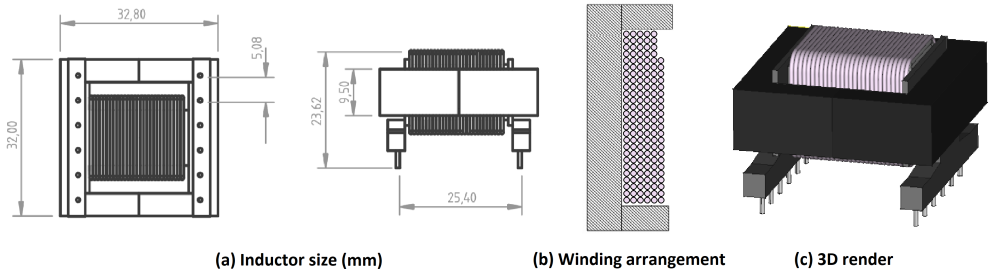

Figure 5-10: Output filter inductor implementation

To measure the inductance and equivalent series resistance (ESR) of L_o and L_s a procedure similar to the transformer measurements were followed. Two ends of the Bode 100 probe were connected to ends of the inductor windings. Moreover, Bode 100 measurements were used to fine tune the airgap to obtain the desired value of the inductance. Inductor measurement results are given in Table 5.4.

Table 5.4: Measurement results for inductors

Parameter	**Value**
Inductance of shim inductor	$\approx 11.3\mu H$
ESR of shim inductor	$\approx 17m\Omega$
Inductance of output filter inductor	$\approx 787\mu H$
ESR of output filter inductor	$\approx 266.35m\Omega$

Chapter 6

Experimental setup and validation

6.1 Open loop

To test the converter performance, it is connected between a constant voltage source and high power rated resistors. Gate driver signals are generated by the SP Card, which is described in the following subsection. Transformer primary and secondary currents are measured using a hall effect current probe, and voltages using high voltage isolated voltage probes. All the measurements are displayed on the oscilloscope. All parts of the modular PCB are mounted on a heatsink, and two stand-alone fans are used to cool down the system, as shown in Figure 6-1.

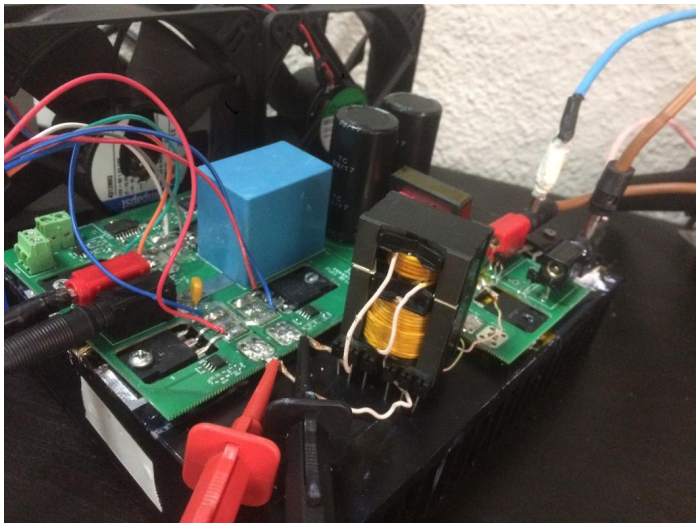

Figure 6-1: Setup of the full power open loop test

6.1.1 SP Card

SP Card was developed at SP Control Technologies, and among other functionality, it allows to generate signals for the driver circuit, and even to drive MOSFETs through a user-friendly software named "SP Tool". Using SP tool one can choose a number of signals to create, their frequency, and also specify deadtime for complementary signals, and a phase shift for signal pairs. These functions made it easy to test the open loop operation of the converter using the parameters obtained from the design and simulation stage. Figure 6-2 from SP Control Technologies official website (http://spcontroltechnologies.com/) shows both the SP Card and the SP Tool.

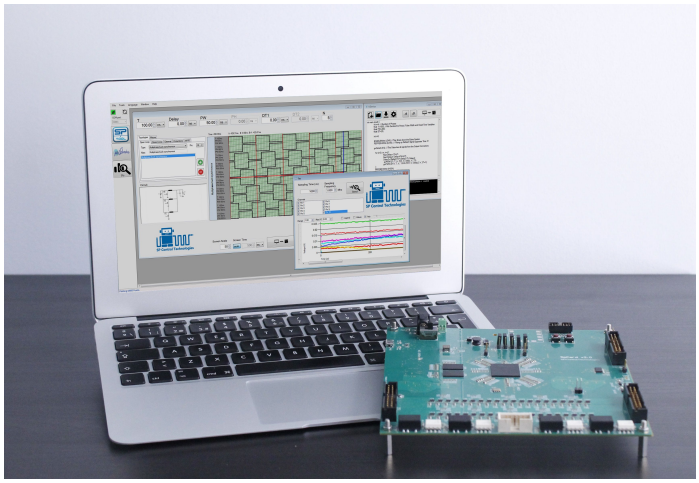

Figure 6-2: SP Card and SP Tool from SP Control Technologies

6.1.2 Design improvements in open loop

All failed versions of the power converter are not covered in the design or implementation process of the thesis. However, it was a very useful learning process since all of these problems were identified during the experimental validation stage, they will be covered in this section.

The first version (PCB-1) was implemented using Texas Instruments Digital Isolator ISO7240MDW with two of UCC27714D High-side Low-side gate drivers (one per leg). However, it was subjected to noise and stopped working at around 20V at the input.

The second version (PCB-2) of the driver was implemented using two half bridge isolators and four gate drivers using a bootstrap circuit. This version of the driver circuit worked well until 50-60V in PSFB converter application, but above that voltage, the EMI noise was causing driver circuit failure. However, it should be noted that this driver circuit worked perfectly well for FB-LLC converter because FB-LLC at rated frequency has the lowest EMI noise. Since the driver circuit was failing, the circuit was tested driving the MOSFETs from SP Card. During these tests, we were able to work up to 150-200V at the input, at which point the rectifier diode on the secondary side was failing. After careful examination, it turned out that instead of expected twice the primary voltage times the turns ratio, the voltage over the rectifier diodes was much higher due to oscillations. At this stage, the parasitic capacitance of the rectifier diodes was not taken into account. The source of oscillations was identified based on several articles, and verified using PSIM simulation. As a first possible solution, the snubber circuit on the secondary side that consists of two diodes and a capacitor has been implemented as a part of PCB-3. The third PCB (PCB-3) had new driver circuit as shown in Figure 5-3, which ended up being used for the final version, and functioned throughout the range of operation. Moreover, the secondary side snubber circuit was added, as shown on Figure 6-3 and silicon carbide (SiC) diodes were used in the rectifier due to their low parasitic capacitance.

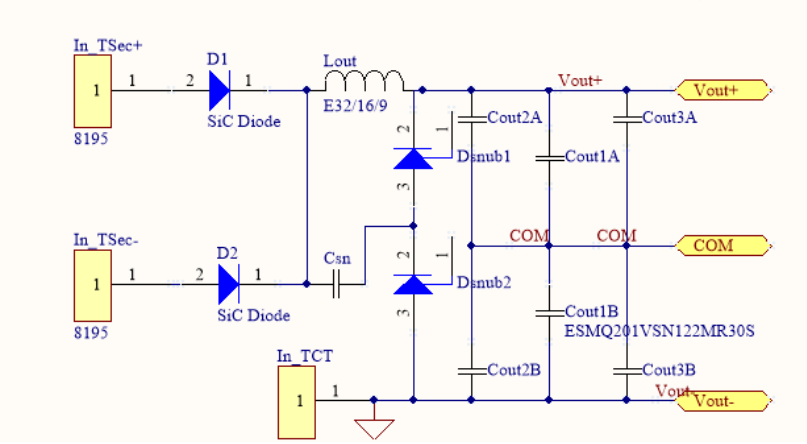

Figure 6-3: Secondary side snubber circuit

This way of implementing snubber decreased the maximum voltage at the recti-

fier diodes from 1650V to 1200-1400V at the rated converter voltages depending on the snubber capacitance value. However, the snubber capacitance was affecting the control of the circuit. Increasing the phase shift (decreasing the effective duty ratio) did not result in the expected change in the output voltage.

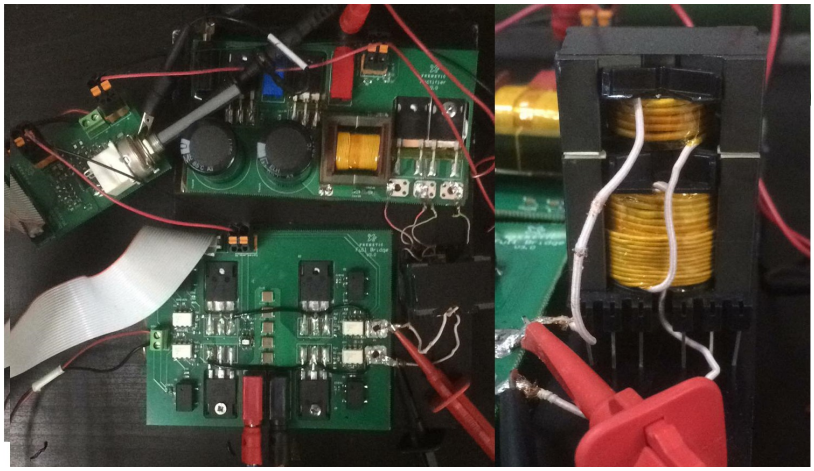

Figure 6-4: PCB-3 using merged transformer and shim inductor

6.1.3 Open loop test at 100% load

The implemented PCB-3 is shown in Figure 6-4. With this version, the open loop performance at the rated power was demonstrated, and the calculated efficiency was approximately 93%. However, after running a couple of successful tests of 30 minutes, there was a short-circuit at the rectifier stage. After a closer examination of the PCB layout, it was discovered that a leg of one of the diodes was within a millimeter distance from a track that had 1.4kV voltage difference from it. For the next iteration, it was taken into account.

Moreover, in PCB-3, the transformer and the shim inductor were merged into one component as shown in Figure 6-4. The design of "mergence" was also performed by Frenetic AI. Mergence is a good alternative to separate magnetic elements since it uses three cores instead of four. However, due to height restrictions of the converter, and the need to use commercially available coil formers, it was decided to use separate inductor and transformer for the final design.

6.2 Closed loop

6.2.1 Design improvements in closed loop

Control system was first tested on PCB-3, as shown in Figure 6-4. Since at this stage, the snubber was on the secondary side, the noise issue was still a problem. For the first test, 150Ω resistor was connected to the converter, voltage setpoint was set to the rated 300V, and input voltage was increased slowly starting at 0V. During the first closed loop test, at around 70V input voltage, the converter was going to the burst mode, which means that one of the full-bridge leg MOSFETs were not receiving any signals from the UCC28950, as shown on the right side part of Figure 6-5. The plots on the left of Figure 6-5 show primary current in light blue, and the CS signal in dark blue. This plot proves that the current measurement circuit works, however, the oscillations due to rectifier diode capacitance pose a big issue for the control.

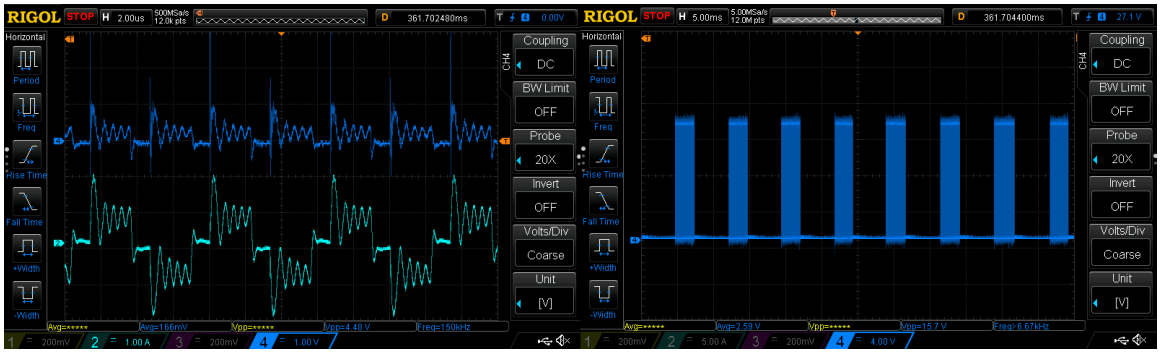

Figure 6-5: PCB-3: Results of the closed loop test

At this stage, several modifications have been done to PCB-3:

- Mergence was replaced by separate transformer and inductor
- Snubber diodes were added at the primary side according to the design described in Chapter 4
- Snubber circuit has been removed from the secondary side
- Extra layers of isolation were added between the diode leg and the track which had 1.4kV voltage difference from it.

- All the "hanging" wires were made as small as possible to decrease noise issue

6.2.2 Closed loop control test

With the improved PCB, which we will denominate as PCB-3A, closed loop test was performed once again. This time results were as in Figure 6-6. The current that flows through the shim inductor is on the left, and the current through the transformer primary side is on the right. Please note that since the input voltage is too low at this point to reach the desired output voltage, the converter is operating at a full duty cycle.

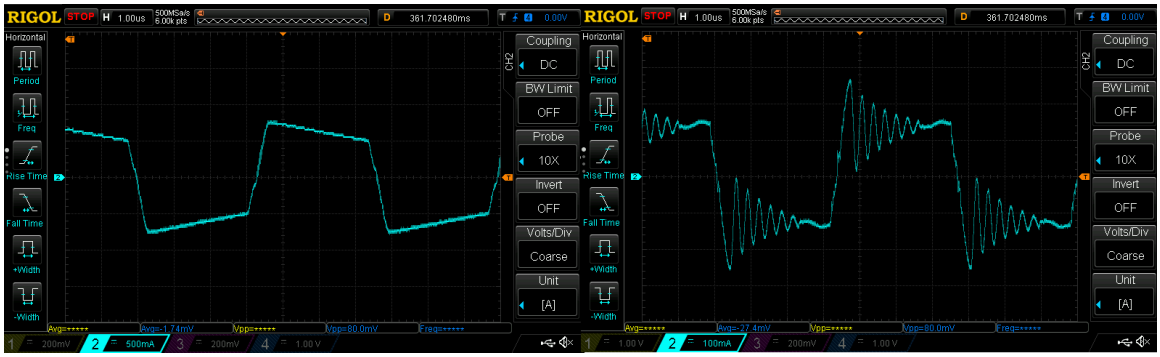

Figure 6-6: PCB-3A: Results of the closed loop test - full duty

To test the control system under safe conditions, the output voltage reference was set to 60V. Figure 6-7 shows the transformer primary side current in light blue and the voltage between the midpoints of two legs (V_{sw}). The control system was able to keep the output voltage at 60V. Tests with this setup were continued up to setpoint of 180V and proved to work (reach desired output voltage), but were subjected to small noise.

One of the tests with 80V input voltage and 55V setpoint is shown in the Figure 6-8. Unfortunately, due to faulty USB port of the oscilloscope, the original image is not available. The green waveform shows the voltage between the midpoints of two half-bridges. The violet plot is a filtered CS signal. The yellow noisy line is the voltage measurement after the voltage divider. The last light blue plot is the primary current. All the waveforms correspond to the expected waveforms obtained through

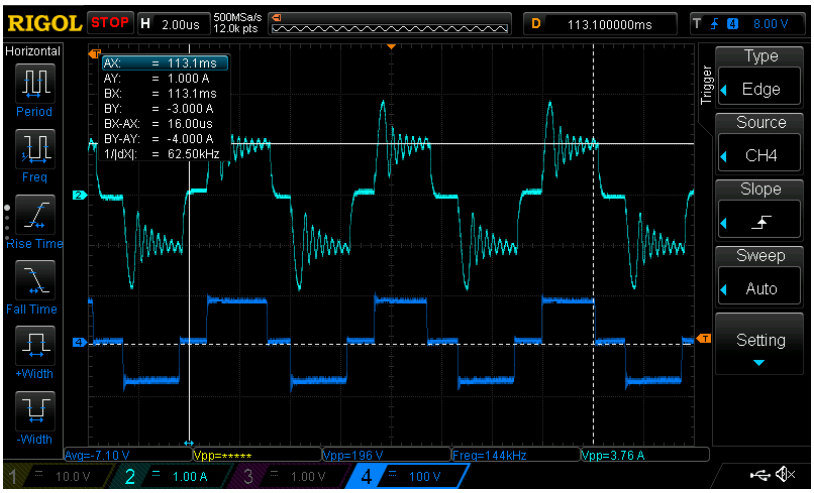

Figure 6-7: PCB-3A: Results of the closed loop test - controlled

simulations.

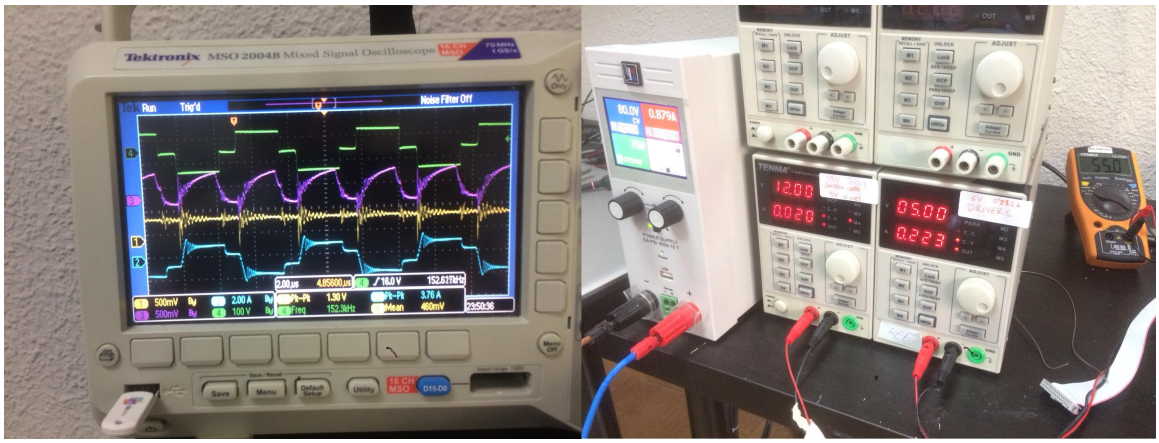

Figure 6-8: PCB-3A: Control waveforms and setup

6.2.3 Bode analyzer loop stability test

Bode 100 analyzer was used to check the stability of the system. The Figure 6-9 demonstrates the test setup for the loop stability test as per instructions given in the application note of Bode 100 [24].

First, the additional resistor $R_{BODE} = 10\Omega$ is connected to the circuit to break the loop and inject a voltage disturbance. The disturbance signal is injected through the B-WIT 100 wideband injection transformer. This signal is then distributed in

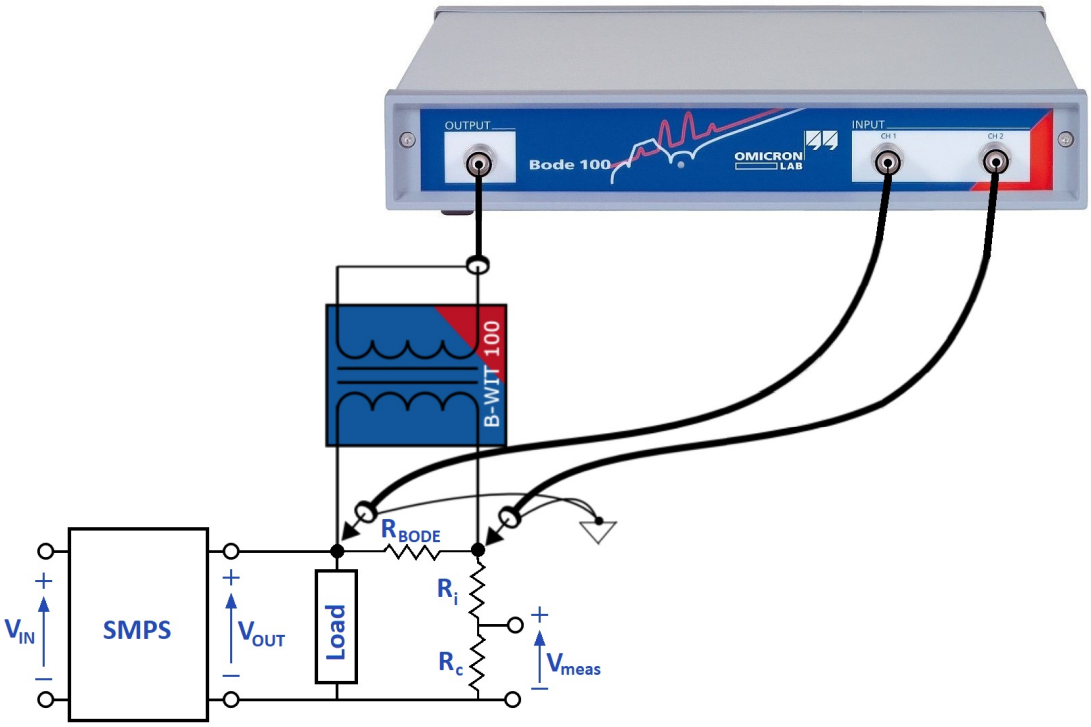

Figure 6-9: Bode analyzer loop stability test setup

the controlled loop, and depending on the loop gain, the signal will be attenuated or amplified and shifted in phase. The results of the test are measured through inputs (CH1 and CH2) of the Bode 100 and then displayed on the Bode 100 software as in Figure 6-11. The loop stability test via injection of voltage disturbance has been performed on the converter at the conditions given in the Table 6.1. The converter was tested in these conditions, rather than the rated ones because measuring loop stability at rated conditions posed a safety hazard due to modifications made to the converter throughout the development.

Table 6.1: Bode analyzer loop stability test conditions

Parameter	**Value**	**Unit**
V_{IN}	120	Volts $[V]$
V_o	100	$[V]$
R_{load}	470	$[k\Omega]$
R_f	470	$[k\Omega]$
C_z	0.27	$[nF]$
C_p	22	$[pF]$

First, the loop gain has been calculated on MATLAB for these operating conditions. Bode plot is demonstrated in Figure 6-10. The loop is stable, the cross-over frequency is 8.26 kHz, the phase margin is 133 degrees, and the gain margin is 14.2dB.

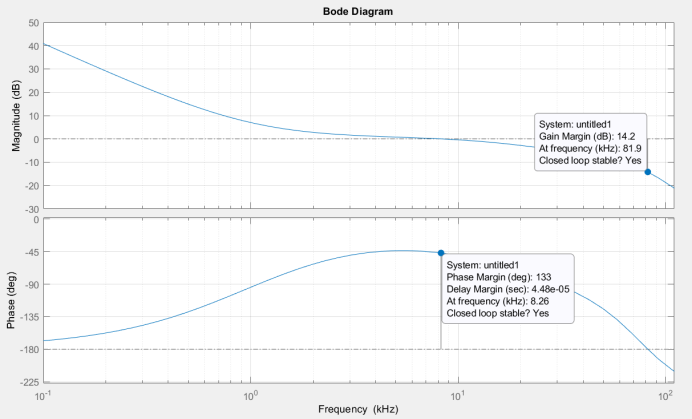

Figure 6-10: Loop stability calculated on MATLAB

Results of the loop stability test on Bode 100 are provided in the Figure 6-11. In Bode 100 plots the phase margin is to be calculated as the distance from zero degrees at the crossover frequency, whereas in standard Bode plot, gain margin is measured from the -180 degrees line.

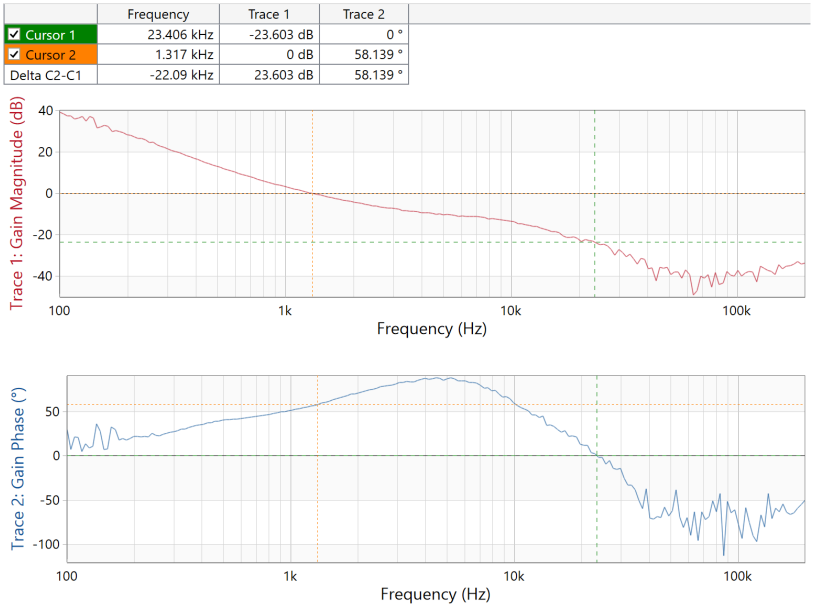

Figure 6-11: Bode analyzer loop stability test results

The crossover frequency is at 1317Hz in contrast to the expected theoretical value

of 8.26kHz, the Phase margin is at 58° instead of 133°, and the gain margin is at 23.6dB instead of expected 14.2dB. At 1317 Hz the gain on MATLAB Bode plot is approximately 2dB. Bode 100 could have registered this frequency as the crossover frequency because of the noise and oscillations due to the nature of SMPS. Moreover, it was discovered that Bode 100 measurements could get affected by grid noise.

6.2.4 Closed loop test at 30% load

As a final test, PCB-3A was tested with 330V at the input and was able to keep the output voltage at 300V, with the total input power of 220W. The load resistor connected during this test is 470Ω. The efficiency at this point is

$$\eta = \frac{V_o^2/R_{load}}{P_{IN}} = \frac{300^2/470}{220} = 87\% \tag{6.1}$$

So the efficiency at roughly a third of the rated load is 87%. Due to the nature of PSFB to achieve the maximum efficiency the converter has to be operated at 50-100% load. Unfortunately, since there have been multiple modifications to this version of the converter, it was not possible to properly fix it on the heatsink, and test it at rated conditions and full power. However, 87% efficiency at 30% load is a sufficiently good result. With all the notes from these tests, the final PCB that is shown in Figure 5-1, and also discussed in Chapters 3-5 has been designed and implemented. This last PCB is still to be fully tested and characterized.

Chapter 7

Conclusion and future work

7.1 Conclusion

A design and implementation of 600W switched-mode power supply with closed loop control has been defined as a key objective of this thesis. To achieve this, seven objectives have been identified in the beginning of this work. The converter has been clearly defined from the customer requirements, thus fulfilling the first objective.

Two of the isolated DC-DC converter topologies with high power density and efficiency, namely, Full-Bridge LLC and Phase-Shifted Full-Bridge have been studied. After the comparative analysis of the aforementioned topologies, PSFB is selected due to its robustness, relatively straightforward control, and ability to work in ZVS over the wide load range. With this, the second objective of this thesis has been accomplished.

Detailed operation of selected Phase-Shifted Full-Bridge converter, along with resonant ZVS considerations has been studied. Based on this study, the third objective of the thesis - design of the PSFB converter has been fulfilled.

To reach the fourth objective of the project, the design was verified through simulations. The PSIM simulations proved to be a very useful tool in improving the design of converter, and simulating the behaviour of parasitic components.

The Phase-shifted full-bridge converter has been implemented, and the fifth objective has been accomplished. The full power open loop test showed 93% efficiency,

whereas the closed loop test at a third of the rated load showed efficiency of 87%. The closed loop test showed that the converter is able to supply constant output voltage, and has a reasonable stability margin and bandwidth, although different than expected from theoretical calculations. With that all of the thesis objectives have been reached.

Unfortunately, zero-voltage switching could not be verified experimentally with the given setup since measuring gate signals and voltage at the MOSFET terminals with isolated probes injects noise into the system, and creates more possibilities for short circuit.

The main value of this thesis is experiencing the entire process of designing and implementing switched-mode power supply. Major challenges of SMPS implementation result mainly from the high-frequency and high-power of the operation. A number of important learning points have been identified through this thesis work:

- Parasitics of the power electronic components are of colossal importance, especially when high-power and high-frequency operation is concerned.
- Isolation of high voltage tracks has to be considered carefully.
- A proper PCB layout can improve the EMI performance and efficiency of the converter.

7.2 Future work

Due to time limitations, some of the functionality of this converter was not properly tested. Moreover, a number of shortcuts and simplifications have been taken during the design process. Therefore there is plenty of possible improvements for this PSFB converter implementation that could be carried out in the future:

- To experimentally validate the converter operation properly, more tests have to be performed at full power in closed loop.

- Converter operation has to be testes with the actual varying load that this power supply is designed for.
- Converter operation has to be tested while connected to the actual PFC rectifier at the input, and not the DC voltage source.
- Proper thermal analysis has to be performed at the design stage to devise a suitable cooling system.
- Synchronous rectification can be explored as an option to increase the efficiency of the converter
- Digital control can potentially be implemented instead of the using commercially available ICs. This would offer more flexibility and more control over the implementation of the control system to adapt it to the requirements of the specific converter.

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